IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 08/886,388
Priority Filing Date ..... July 1, 1997
Inventor ..... Gurtej S. Sandhu et al.
Assignee ..... Micron Technology, Inc.
Priority Group Art Unit 2811
Priority Examiner ..... Sara W. Crane
Attorney's Docket No. MI22-1736
Title: Method of Forming a Capacitor and a Capacitor Construction

PRELIMINARY AMENDMENT

To: Assistant Commissioner for Patents
Washington, D.C. 20231

From: Frederick M. Fliegel, Ph.D.
(Tel. 509-624-4276; Fax 509-838-3424)
Wells, St. John, Roberts, Gregory & Matkin P.S.
601 W. First Avenue, Suite 1300
Spokane, WA 99201-3817

Sir:

This is a preliminary amendment accompanying a Request for Continuation Application for the above-entitled patent application. Prior to examining the application, please enter the following amendments.

AMENDMENTS

In the Specification

At page 1, after the title, insert:

CROSS REFERENCE TO RELATED APPLICATION

This patent application is a Continuation of U.S. Patent Application Serial No. 08/886,388 filed July 16, 1997, entitled "Method of Forming a Capacitor and a Capacitor Construction", naming Gurtej S. Sandhu and Pierre C. Fazan as inventors, which is a divisional application of United States Patent Application Serial No. 08/582,385, which was filed January 3, 1996, now U.S. Patent No. 6,218,237.

In the Claims

Cancel claims 1-45 and add new claims 46-60 as shown below.

New Claims

46. A pair of adjacent stacked capacitors fabricated on a semiconductor substrate, the adjacent stacked capacitors respectively each including:

a polycrystalline silicon lower plate, the lower plates having a minimum lateral spacing from one another that is less than a minimum photolithographic feature dimension with which the capacitors are fabricated; and

a plug extending below the plate and having a diameter less than the minimum photolithographic feature dimension.

47. The pair of capacitors of claim 46, wherein each plug comprises polysilicon and extends through the plate.

48. The capacitors of claim 46, wherein the lower plates are formed from conductive polysilicon.

49. The pair of capacitors of claim 46, wherein the pair of stacked capacitors are coated with a capacitor dielectric layer.

50. A pair of adjacent stacked capacitors fabricated on a semiconductor substrate using a process having a characteristic minimum lithographic feature dimension, the adjacent stacked capacitors respectively including a lower plate having a minimum lateral spacing from one another which is less than the minimum lithographic feature dimension, wherein each of the pair of capacitors comprises:

a plug having a diameter less than the minimum lithographic feature dimension; and

in cross-section, at least two laterally opposed fins interconnected with and projecting laterally from the plug.

51. The pair of capacitors of claim 50, wherein the plug and fins are formed from conductive polysilicon.

52. The pair of capacitors of claim 50, wherein the pair of stacked capacitors are coated with a capacitor dielectric layer.

53. A pair of adjacent stacked capacitors fabricated on a semiconductor substrate using a lithographic process having a characteristic minimum lithographic feature dimension, the adjacent stacked capacitors respectively including a lower plate having a minimum lateral spacing from one another which is less than the minimum lithographic feature dimension, each lower plate comprising a conductive plug having a diameter less than the minimum lithographic feature dimension, and, in cross-section, at least two laterally opposed fins interconnected with and projecting laterally from the plug.

54. The pair of capacitors of claim 53, wherein the plug includes a minimum width which is less than the minimum lithographic feature dimension.

55. The pair of capacitors of claim 53, wherein the plug and fins are formed from conductive polysilicon.

56. The pair of capacitors of claim 53, wherein the pair of stacked capacitors are coated with a capacitor dielectric layer.

57. A pair of adjacent stacked capacitors fabricated on a semiconductor substrate using a lithographic process having a characteristic minimum lithographic feature dimension, the adjacent stacked capacitors respectively including a finned lower plate having a minimum lateral spacing from one another which is less than the minimum lithographic feature dimension, wherein each finned lower plate comprises:

a conductive plug; and

in cross-section, at least two laterally opposed fins interconnected with and projecting laterally from the plug, the plug having a minimum width which is less than the minimum lithographic feature dimension.

58. The pair of capacitors of claim 58, wherein the plug and lower plates are formed from conductive polysilicon.

59. The pair of capacitors of claim 58, wherein the plug and fins are formed from conductive polysilicon.

60. The pair of capacitors of claim 58, wherein the pair of stacked capacitors are coated with a capacitor dielectric layer.

REMARKS

Claims 1-45 have been canceled and new claims 46-60 have been added.

New claims 46-60 are supported at least by p. 4, line 5 through p. 13, line 3 of the application as originally filed. No new matter is added by new claims 46-60.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page(s) are captioned "**Version with markings to show changes made**."

This application is believed to be in condition for allowance and action to that end is requested. The Examiner is requested to telephone the undersigned in the event that the next office action is one other than a Notice of Allowance. The undersigned is available during normal business hours (Pacific Time Zone).

Respectfully submitted,

Dated: June 6, 2001 By: _____

Frederick M. Fliegel, Ph.D.
Reg. No. 36,138

Version with markings to show changes made.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 08/886,388
Priority Filing Date ..... July 1, 1997
Inventor ..... Gurtej S. Sandhu et al.
Assignee ..... Micron Technology, Inc.
Priority Group Art Unit 2811
Priority Examiner ..... Sara W. Crane
Attorney's Docket No. MI22-1736
Title: Method of Forming a Capacitor and a Capacitor Construction

37 CFR §1.121(b)(1)(iii) AND 37 CFR §1.121(c)(1)(ii) FILING REQUIREMENTS TO ACCOMPANY PRELIMINARY AMENDMENT

Deletions are bracketed, additions are underlined.

In the Specification

At page 1, after the title, the following was inserted:

CROSS REFERENCE TO RELATED APPLICATION

This patent application is a Continuation of U.S. Patent Application Serial No. 08/886,388 filed July 16, 1997, entitled "Method of Forming a Capacitor and a Capacitor Construction", naming Gurtej S. Sandhu and Pierre C. Fazan as inventors, which is a divisional application of United States Patent Application Serial No. 08/582,385, which was filed January 3, 1996, now U.S. Patent No. 6,218,237.

END OF DOCUMENT

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Priority Filing Date . . . . . July 1, 1997
Inventor . . . . . Gurtej S. Sandhu et al.
Assignee . . . . . Micron Technology, Inc.
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TITLE: Method of Forming a Capacitor and a Capacitor Construction

Assistant Commissioner for Patents
Washington, D. C. 20231
Attention: Official Draftsman

SUBSTITUTE DRAWING REQUEST

Enclosed are Red-line drawings of Figs. 1-22 along with corrected substitute formal drawings. Please enter the enclosed substitute formal drawings in the above-referenced application in place of drawings originally filed. The content of the drawings are identical to those now on file in this application.

Acknowledgment of receipt of the formal drawings and their acceptance into the file is requested.

Respectfully submitted,

Date: June 6, 2001

By: _____

Frederick M. Fliegel, Ph.D.
Reg. No.: 36,138
WELLS, ST. JOHN, ROBERTS,
GREGORY & MATKIN P.S.
601 W. First Avenue, Suite 1300
Spokane, WA 99201-3828
(509) 624-4276

Enclosures: 12 sheets of Red-line Drawings, Figs. 1-22 and 12 Sheets of Formal Drawings, Figs. 1-22.

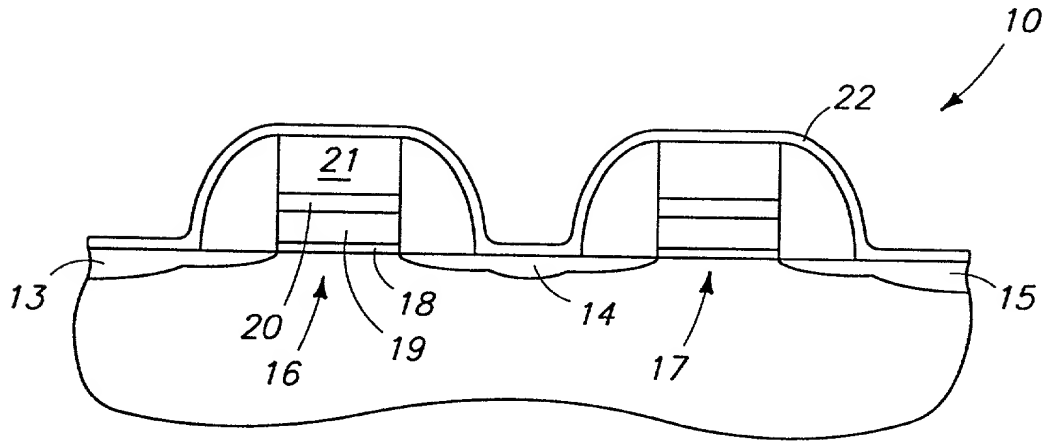

FIG 1

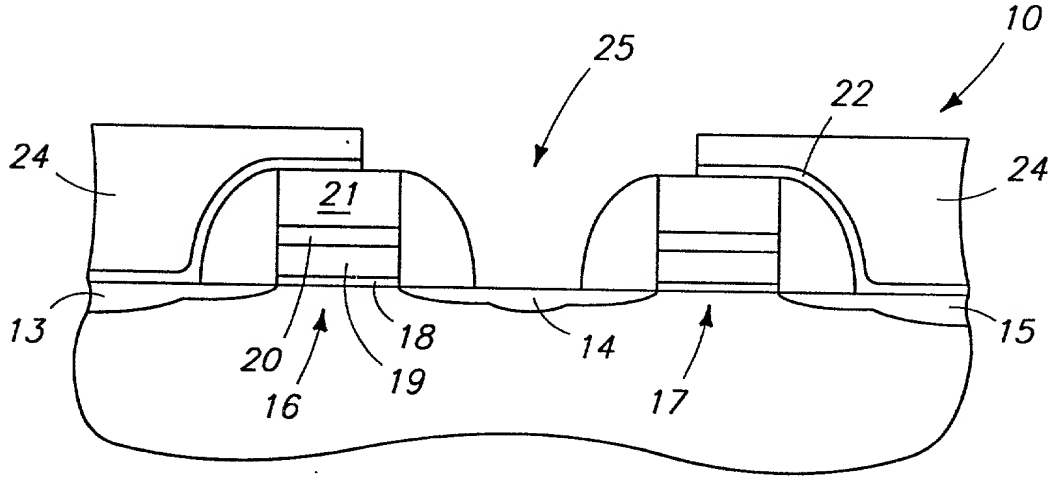

FIG 2

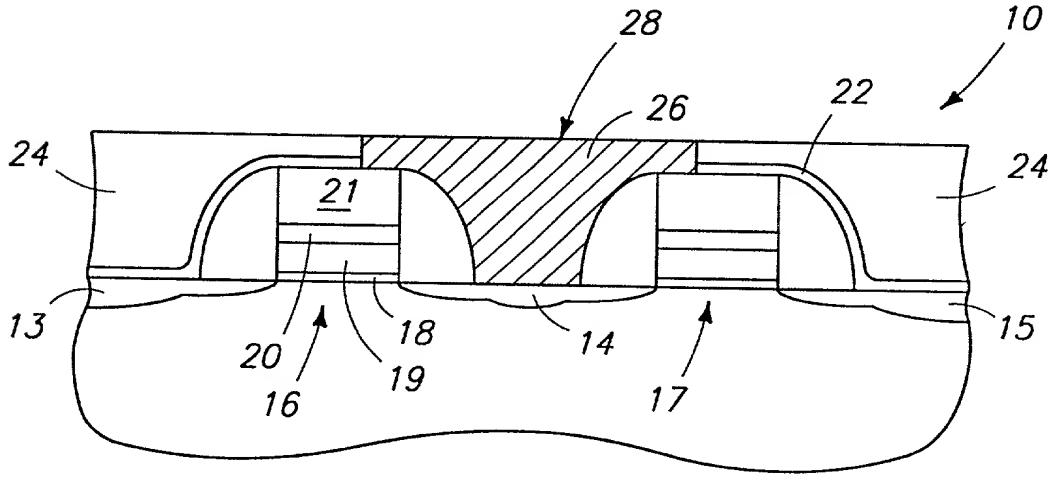

FIG 3

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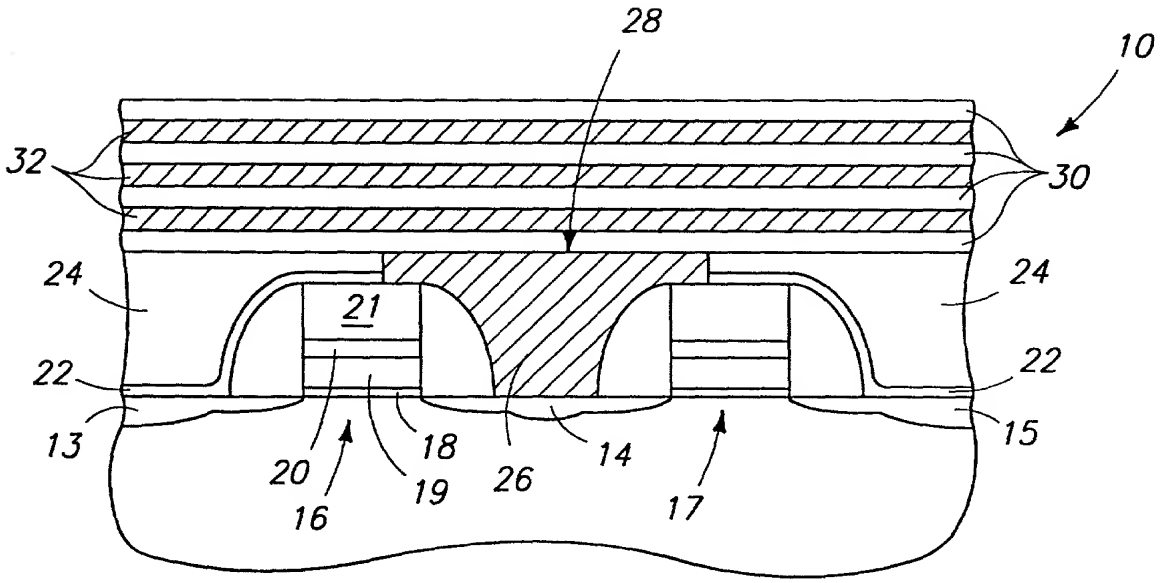

Fig 4

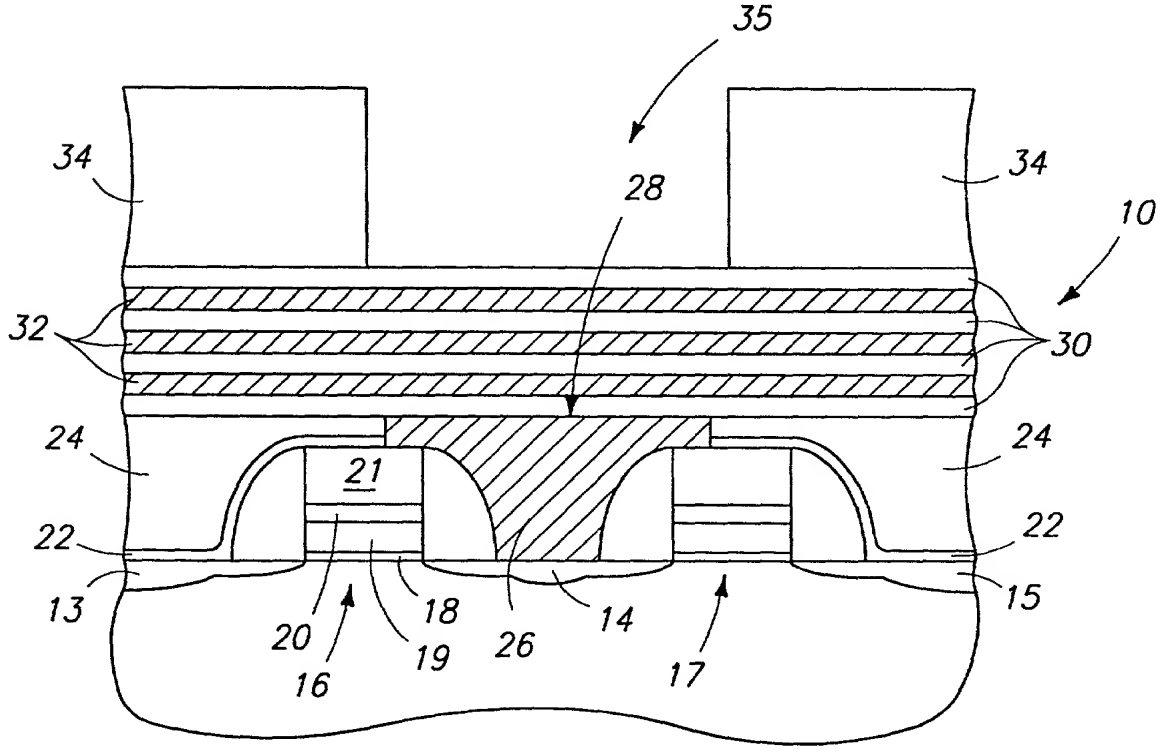

Fig 5

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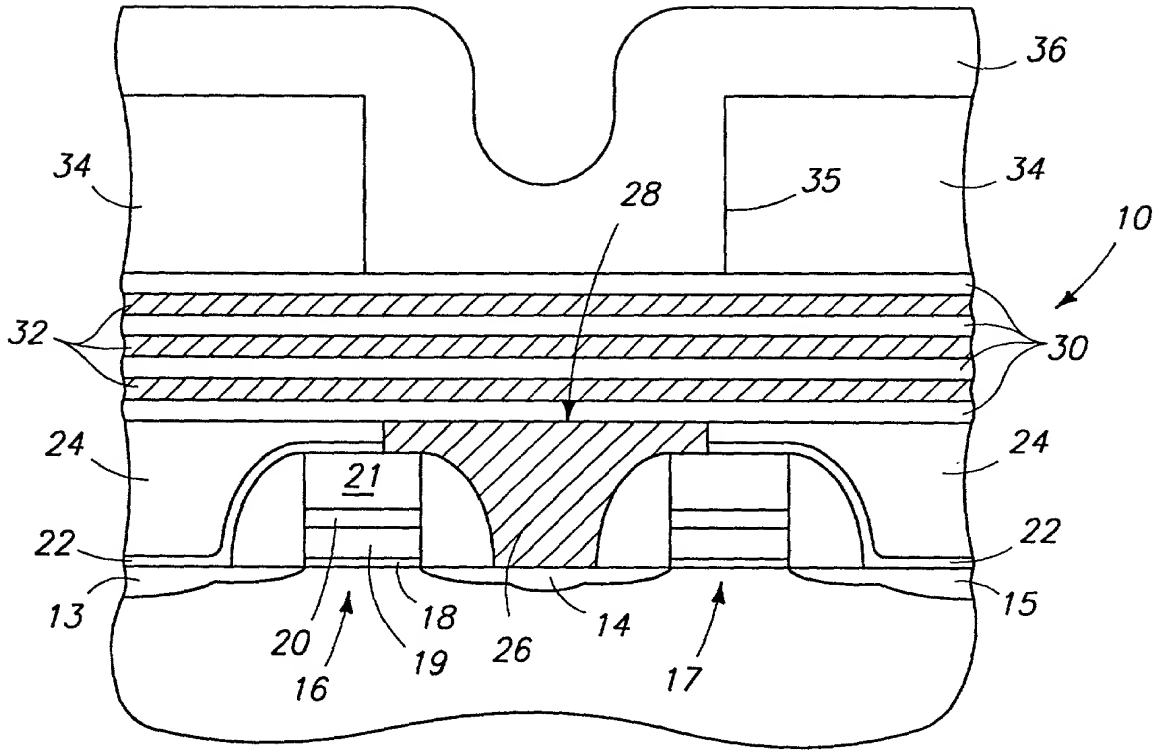

Fig 6

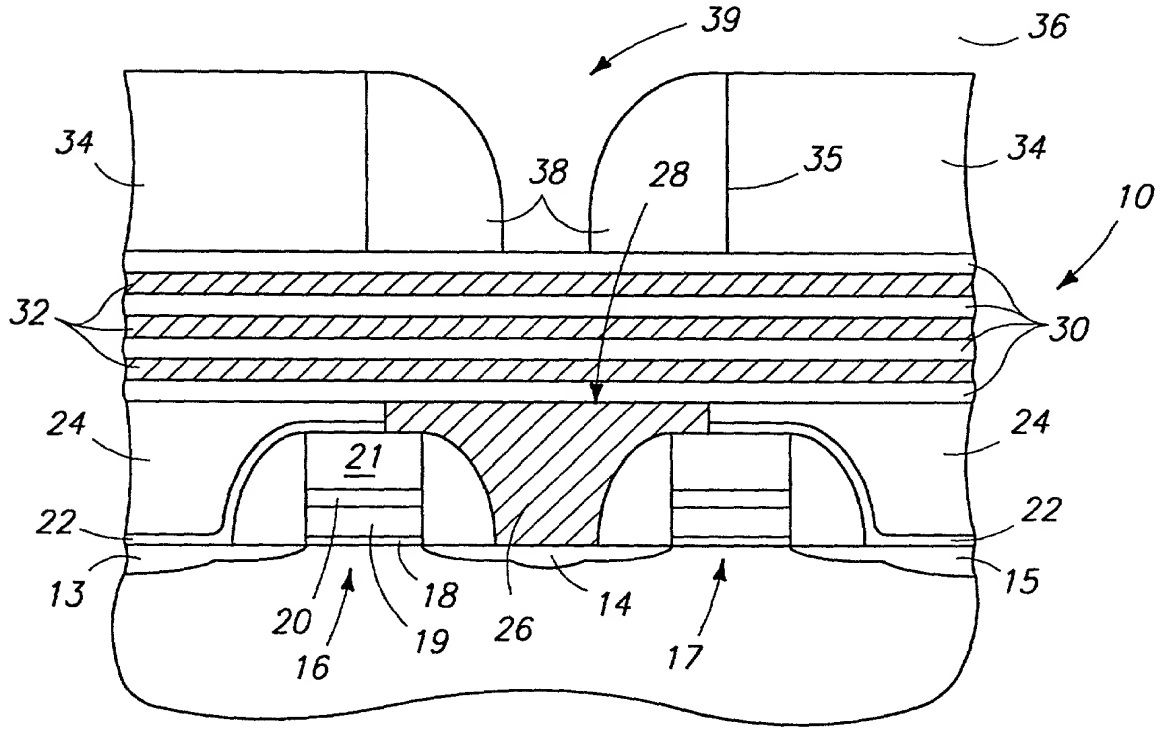

Fig 7

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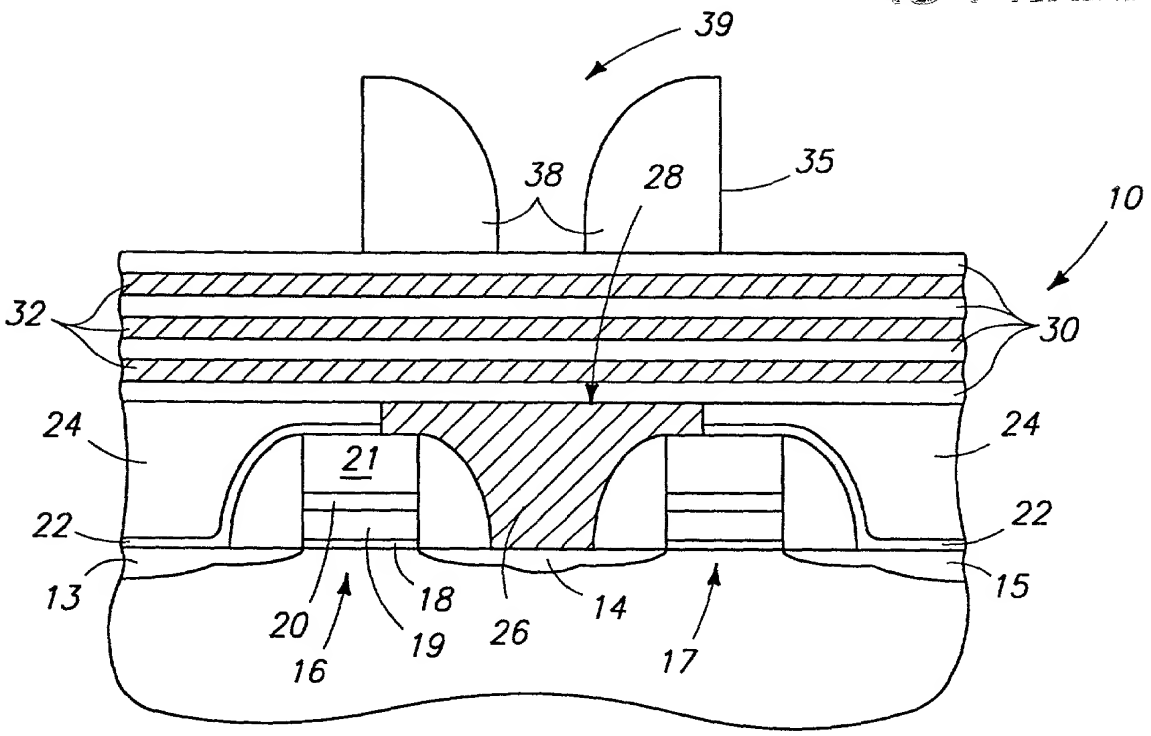

Fig 8B

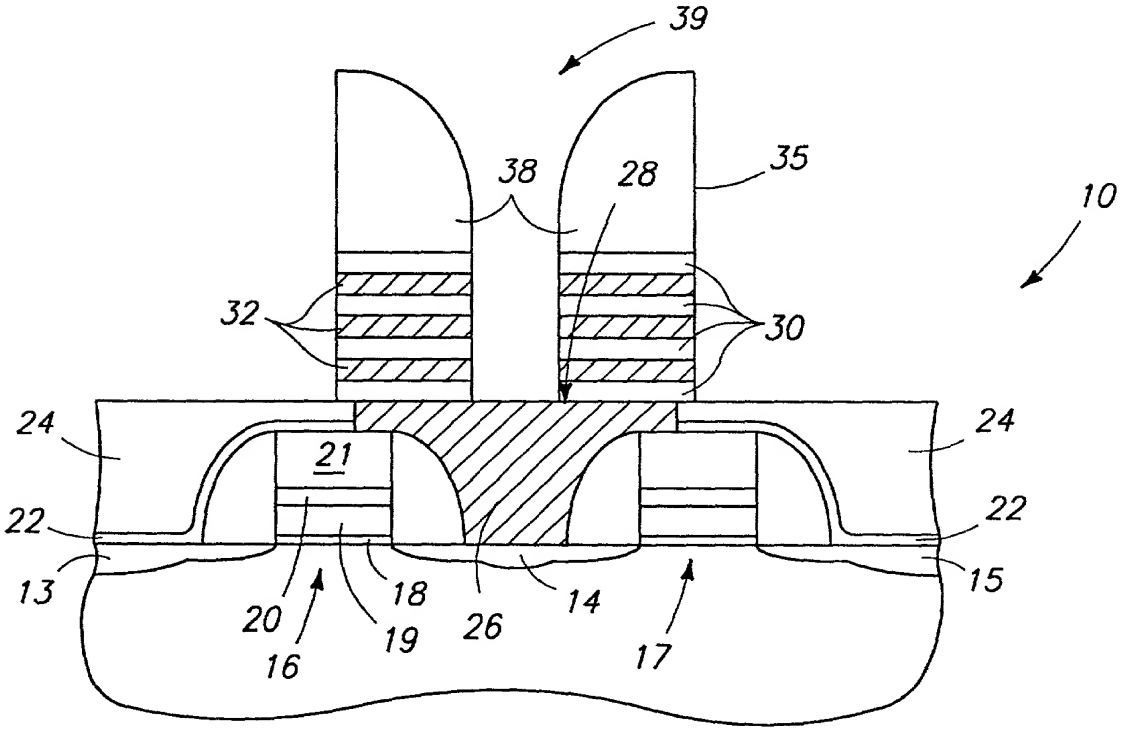

Fig 9

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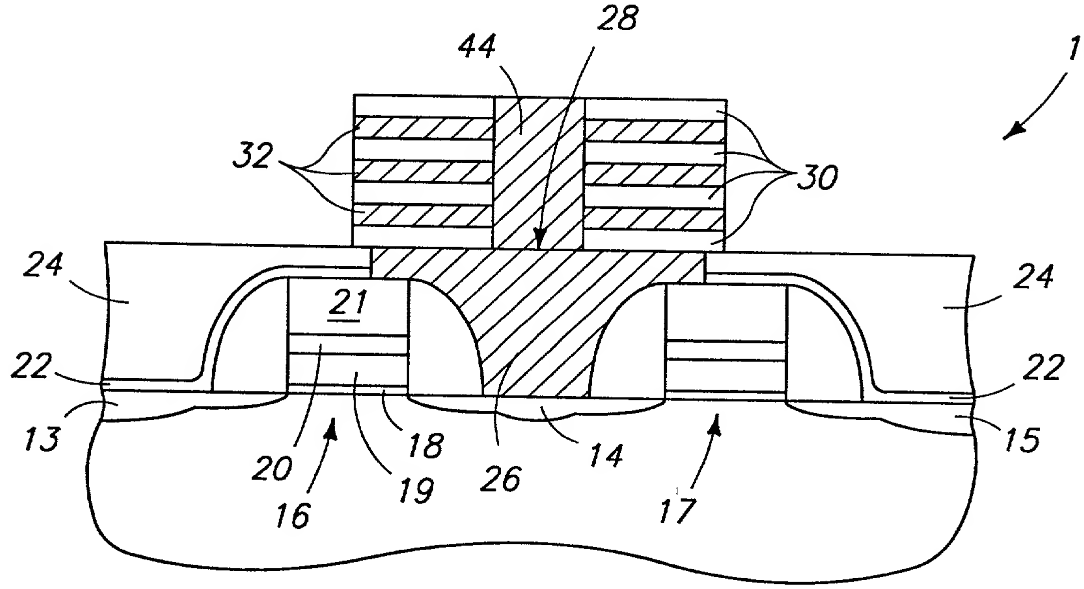

Fig 10

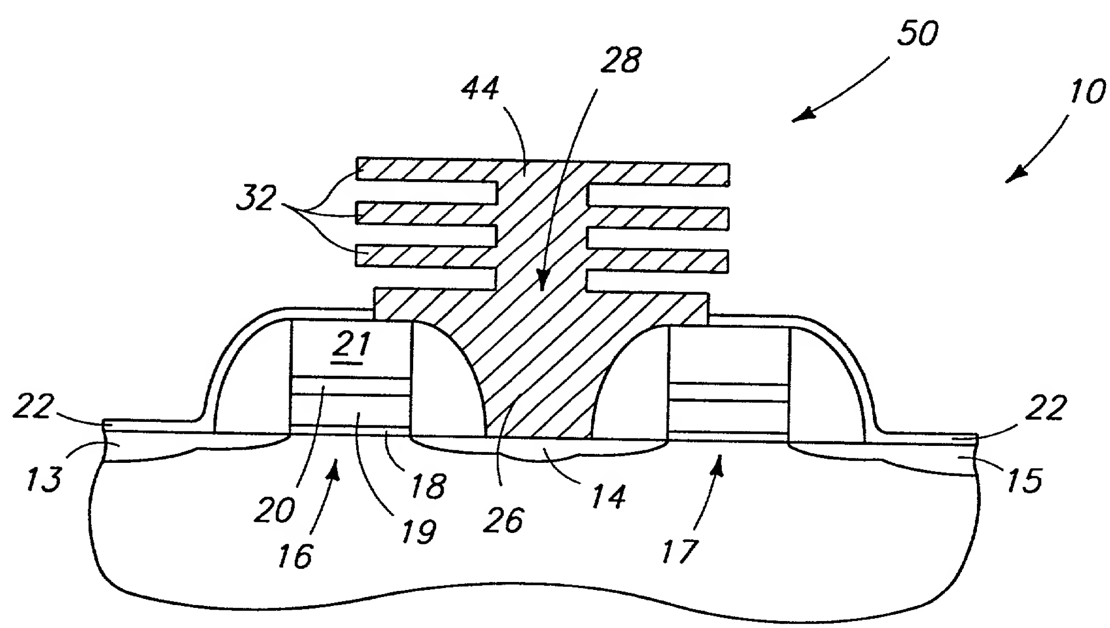

Fig 11

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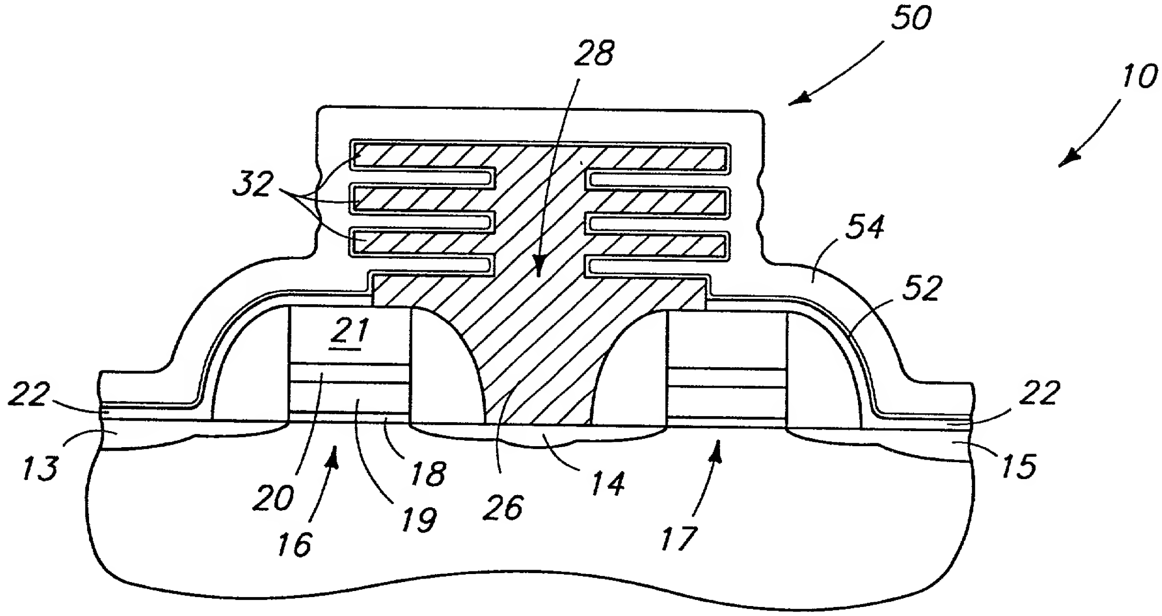

Fig 12

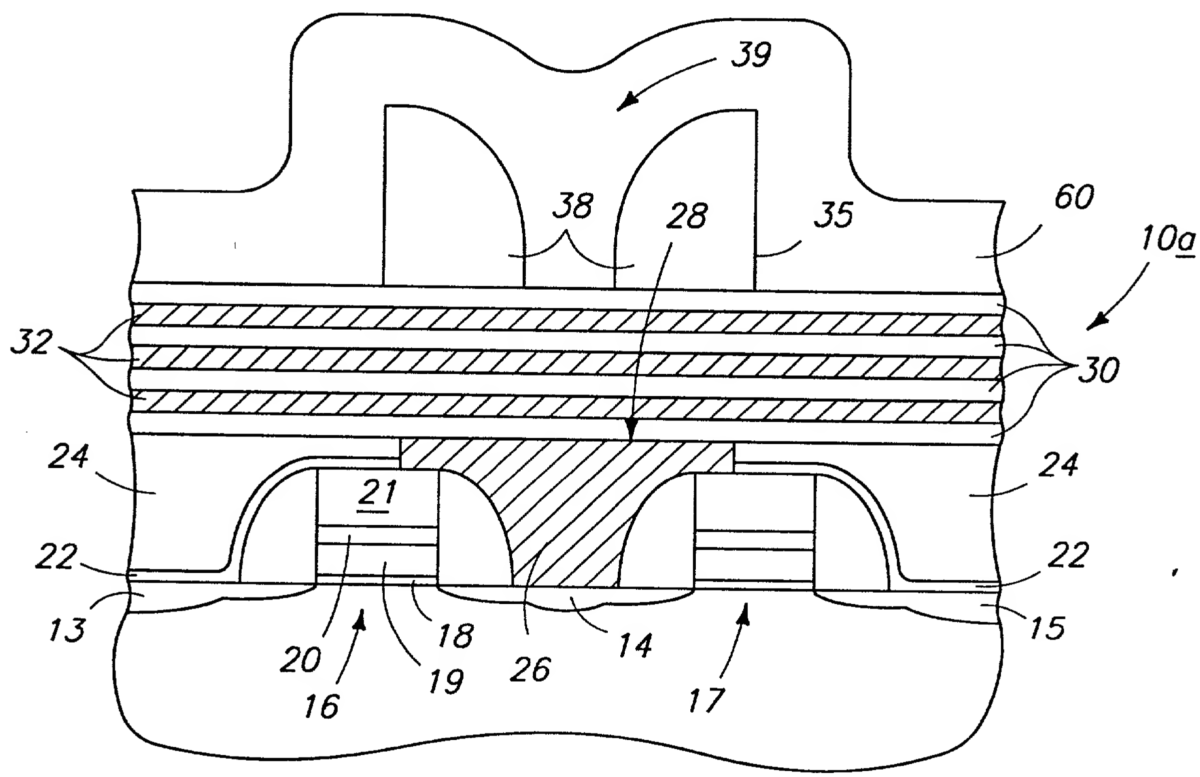

Fig 13

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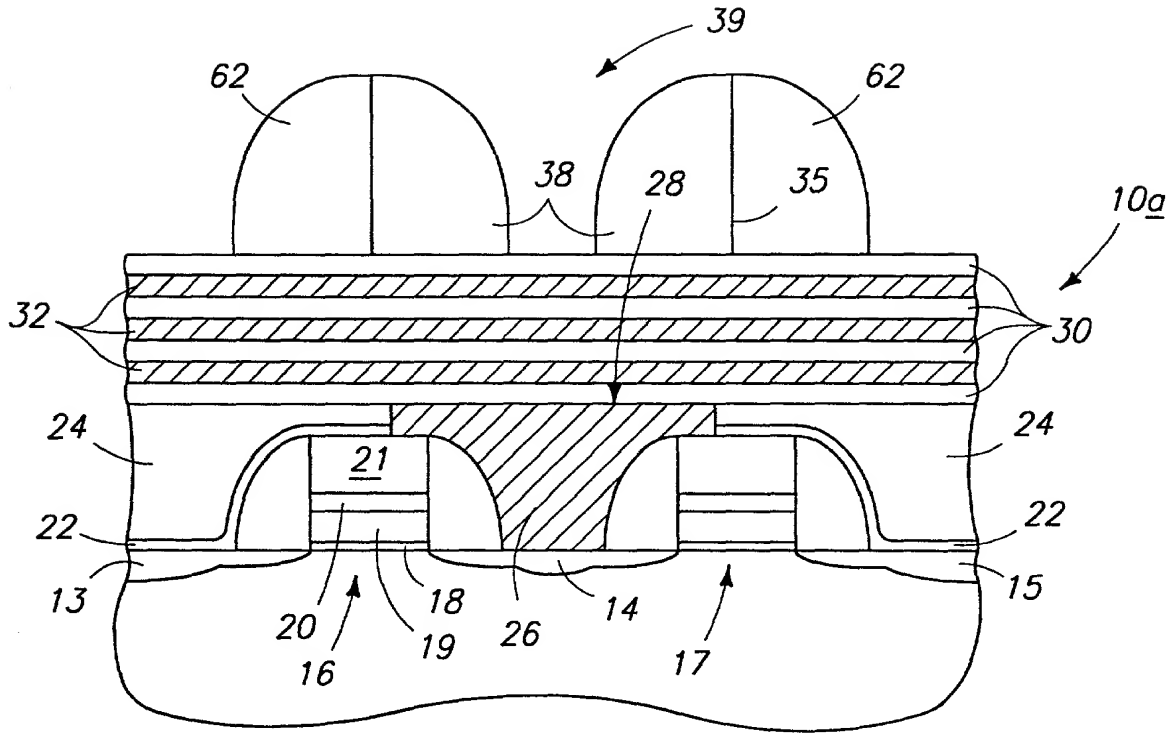

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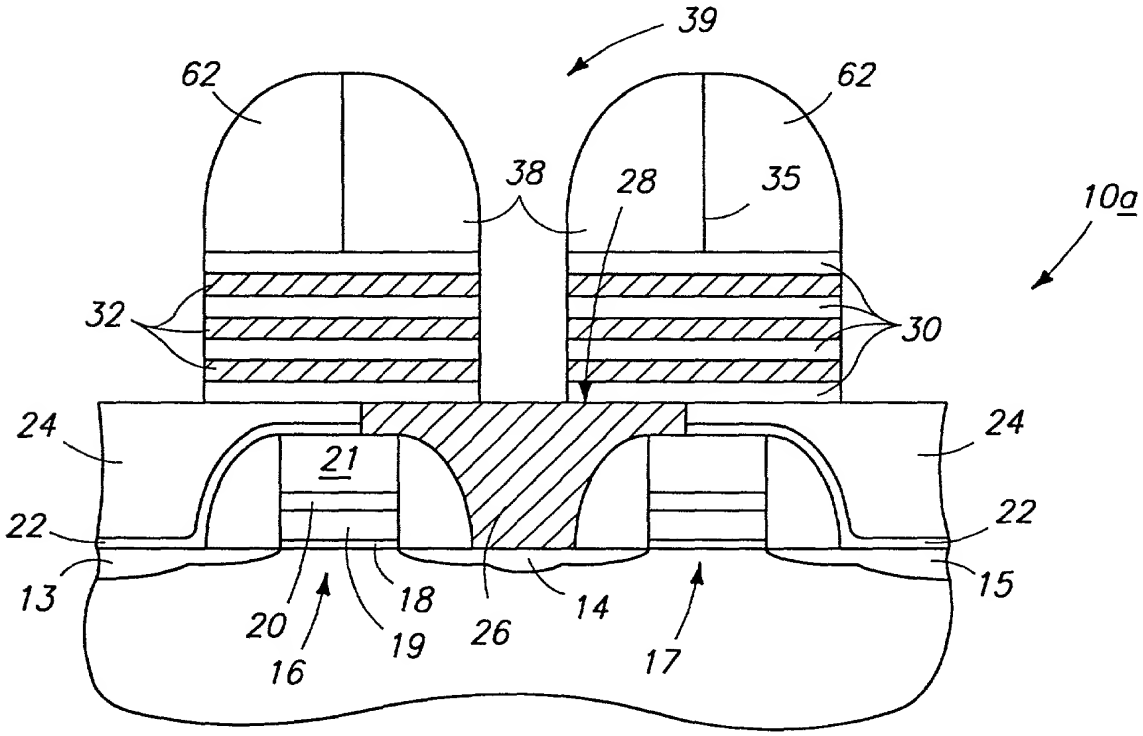

Fig 15

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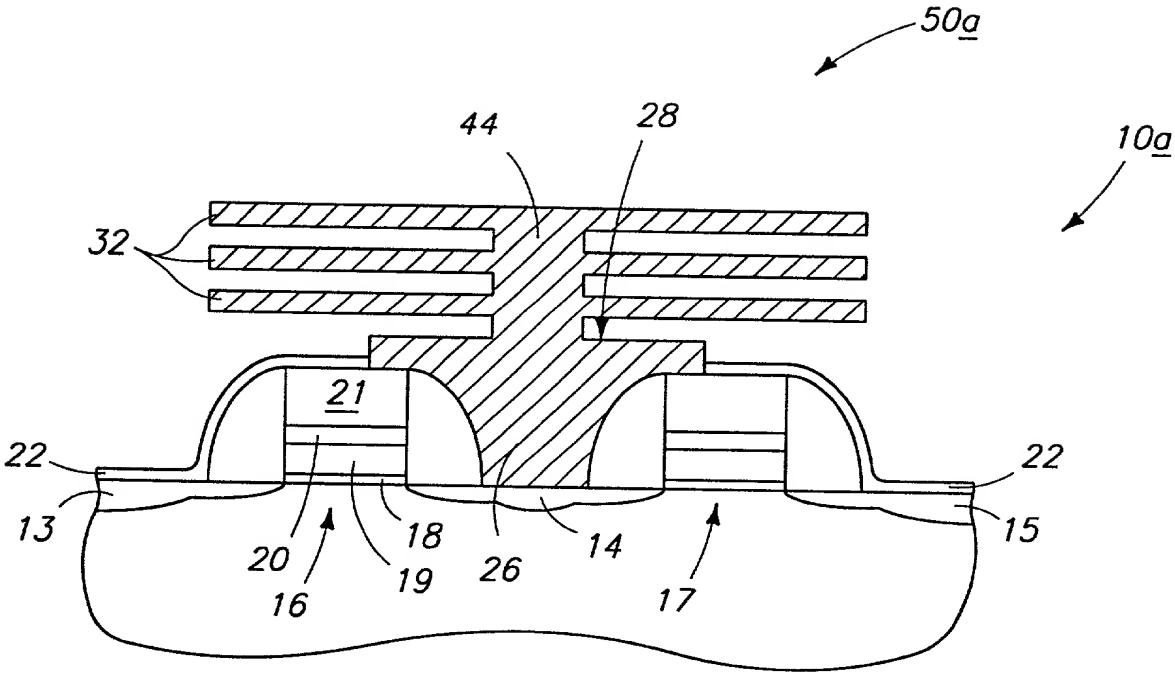

Fig 16

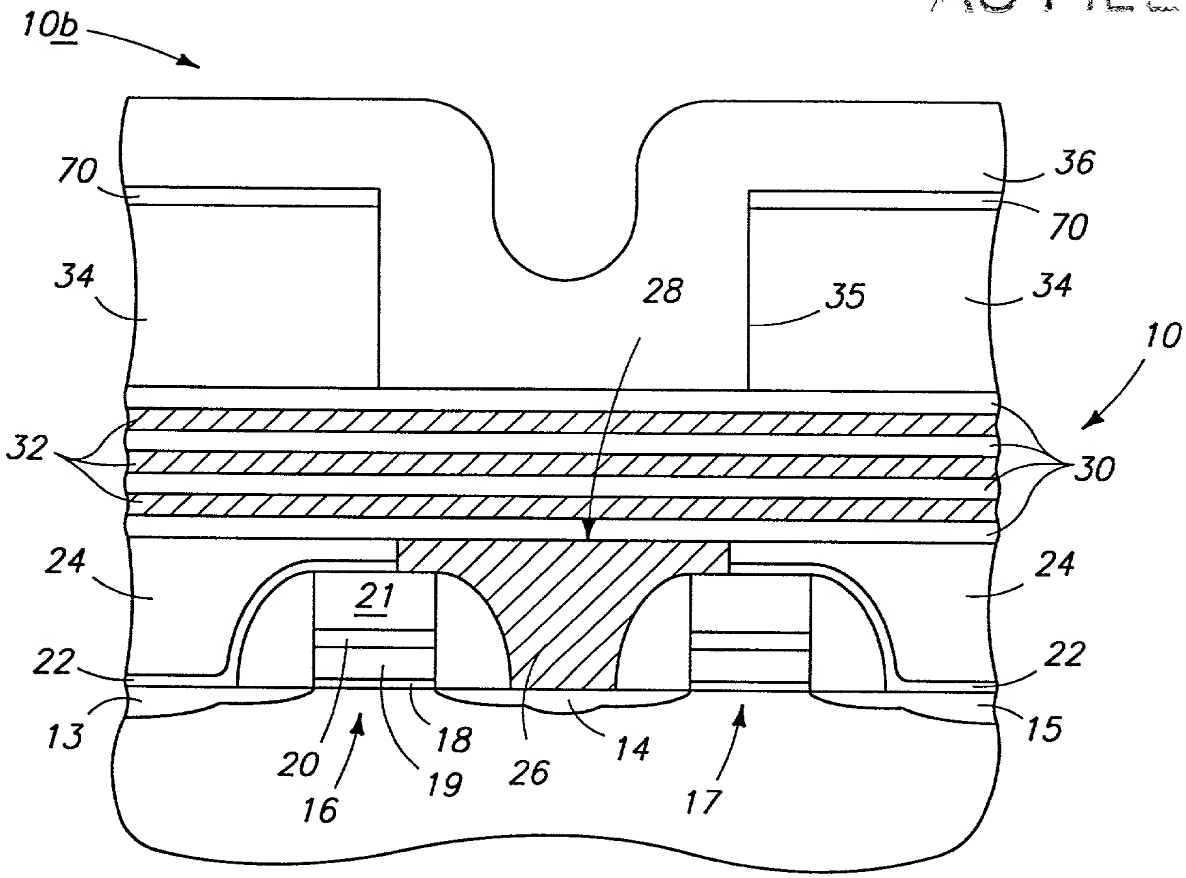

Fig 17

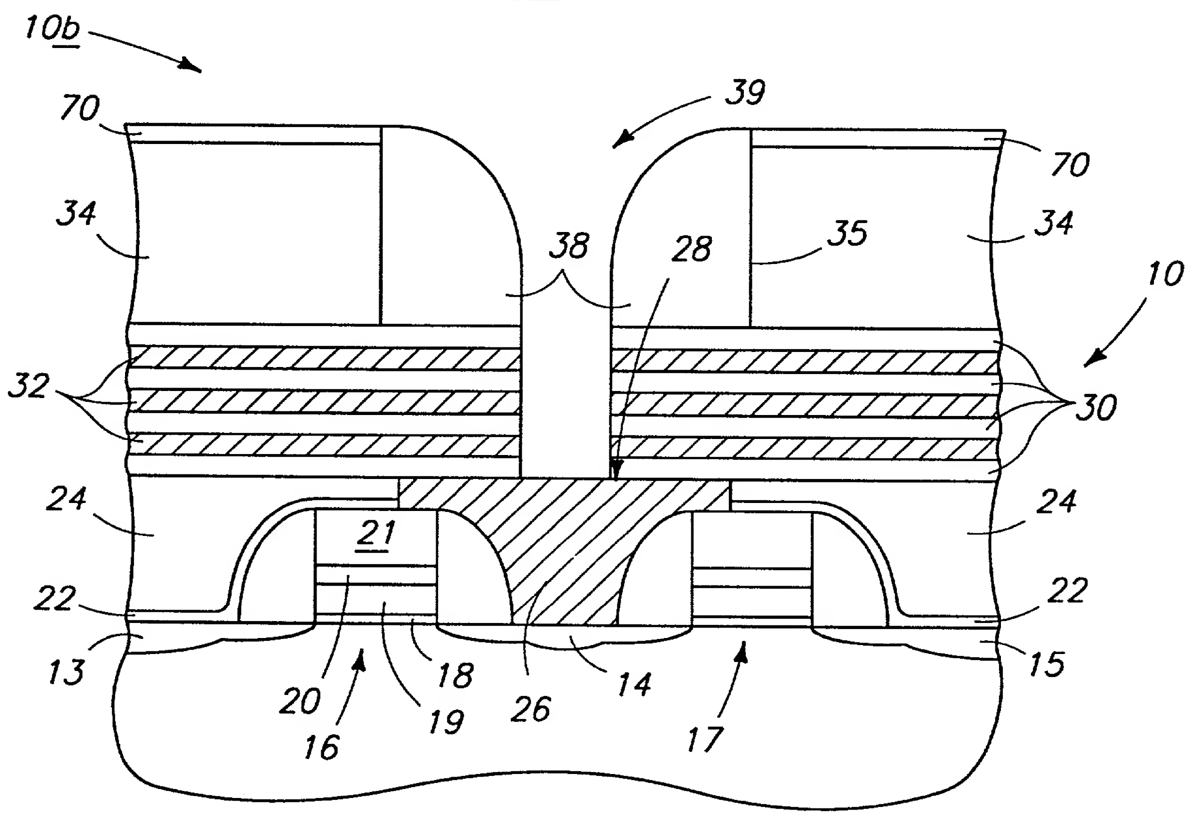

Fig 18

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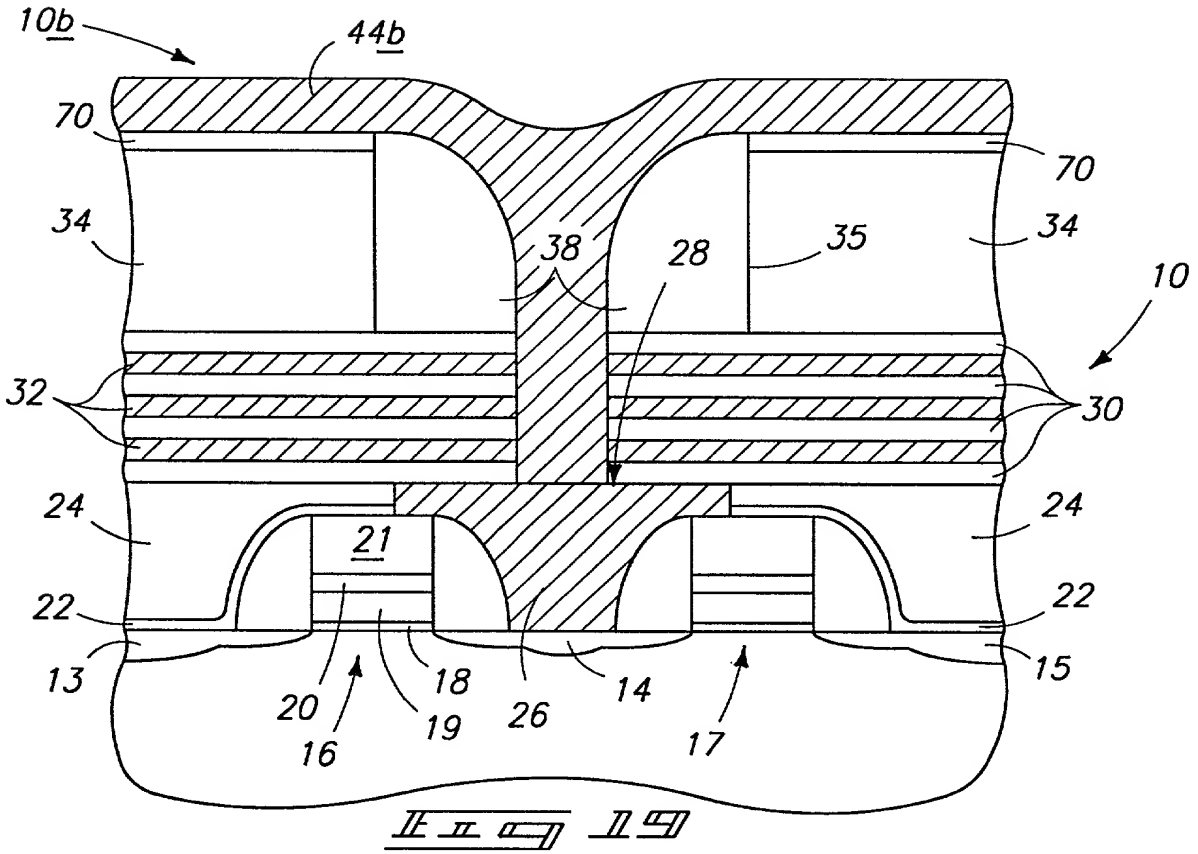

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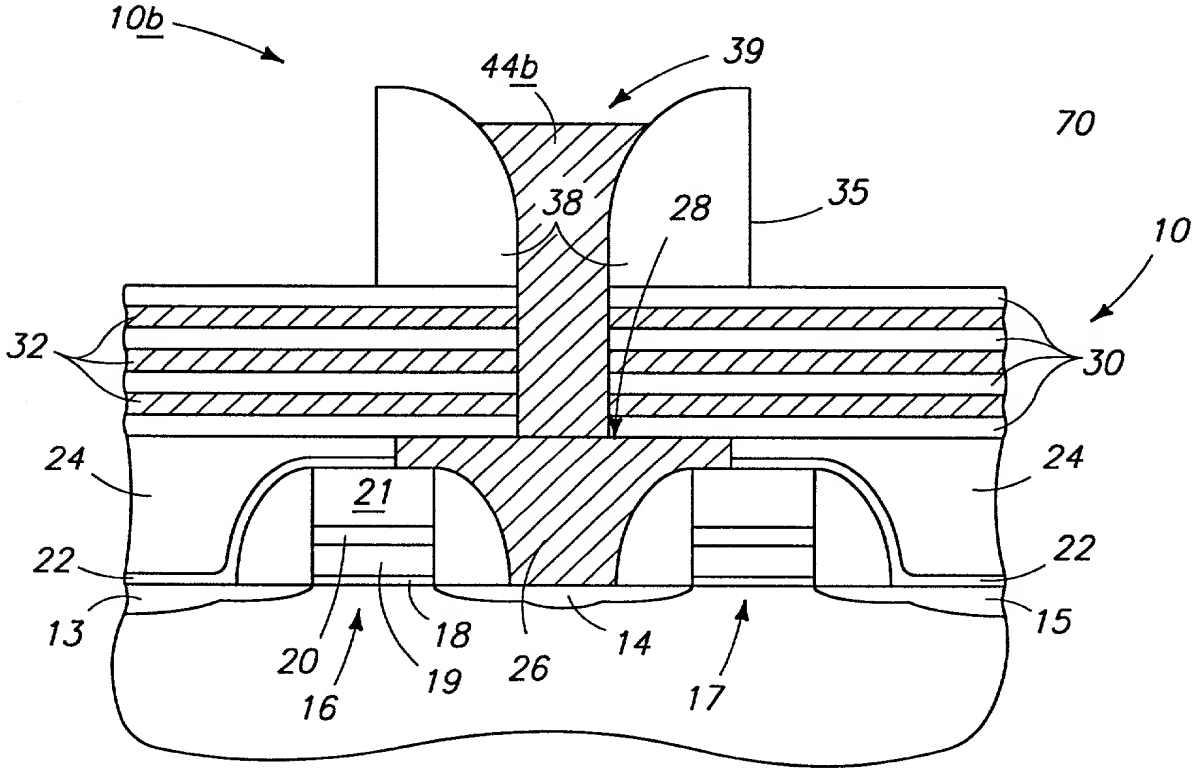

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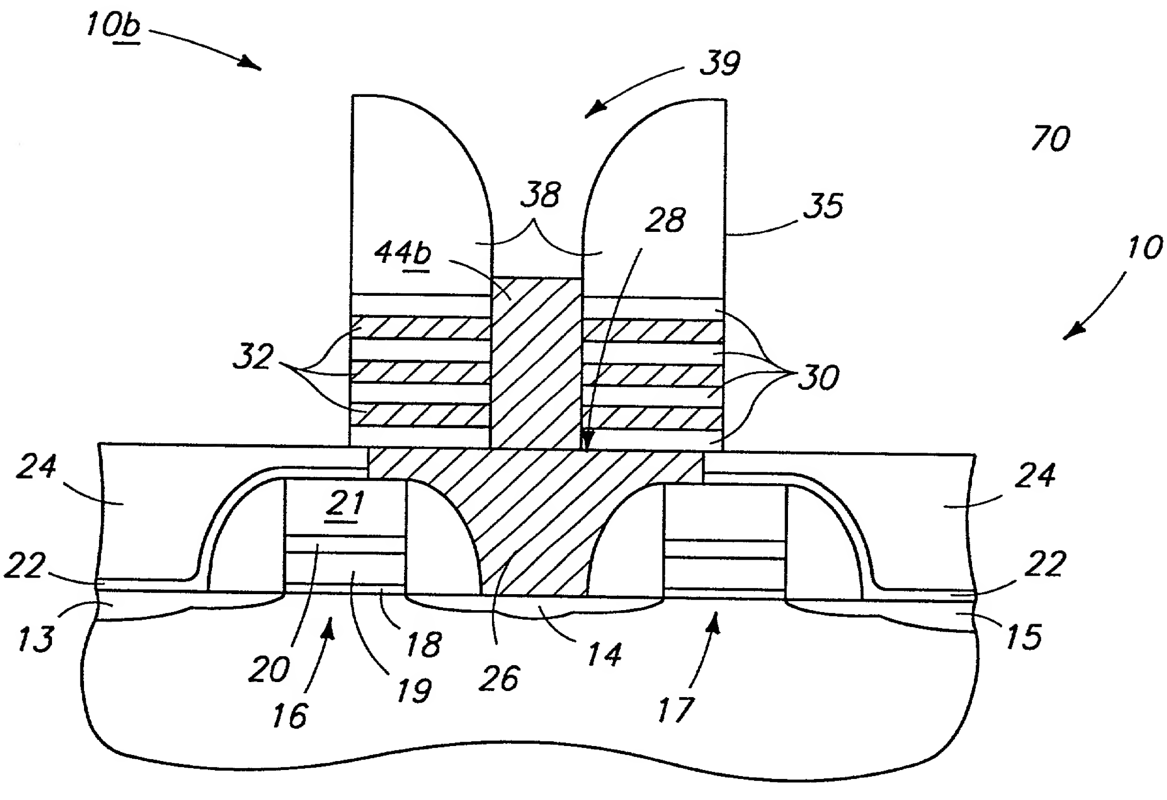

Fig 21

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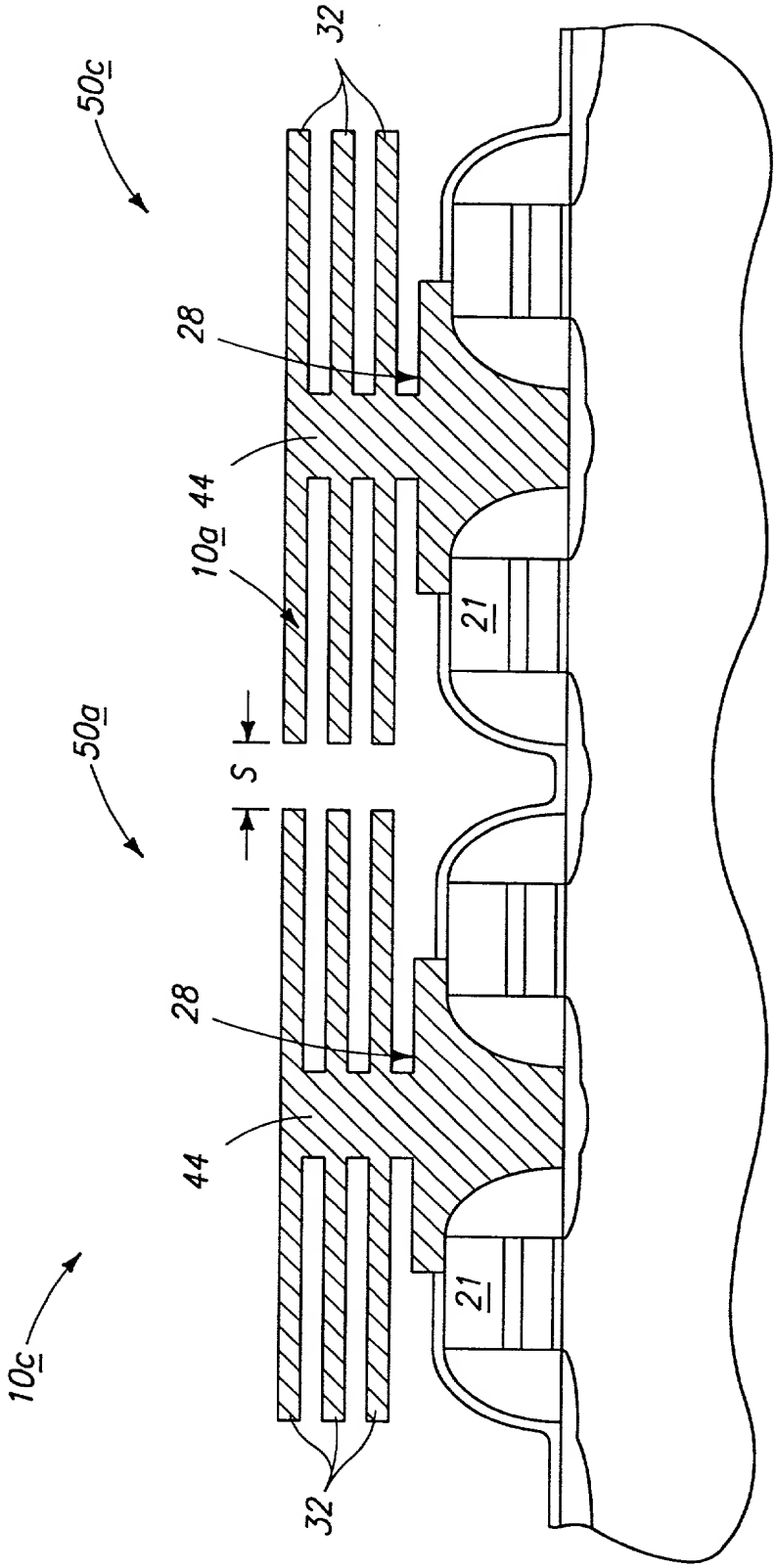

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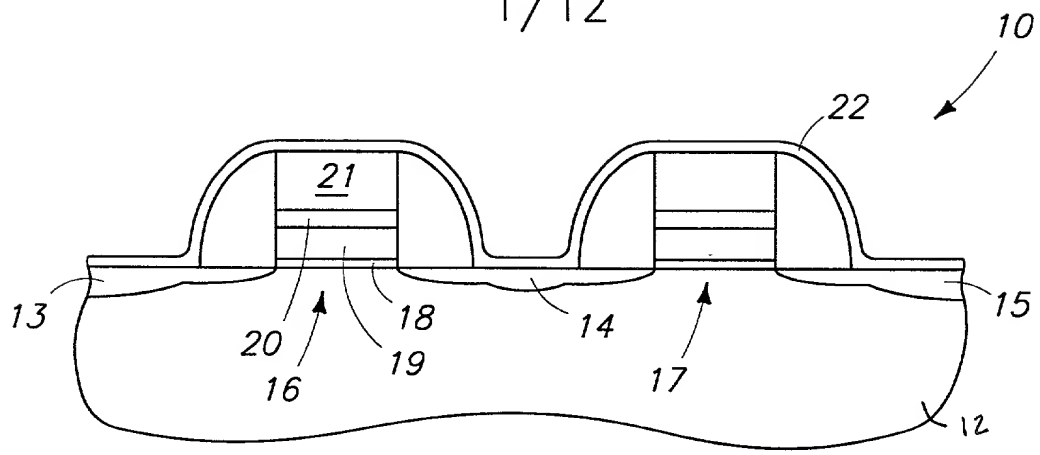
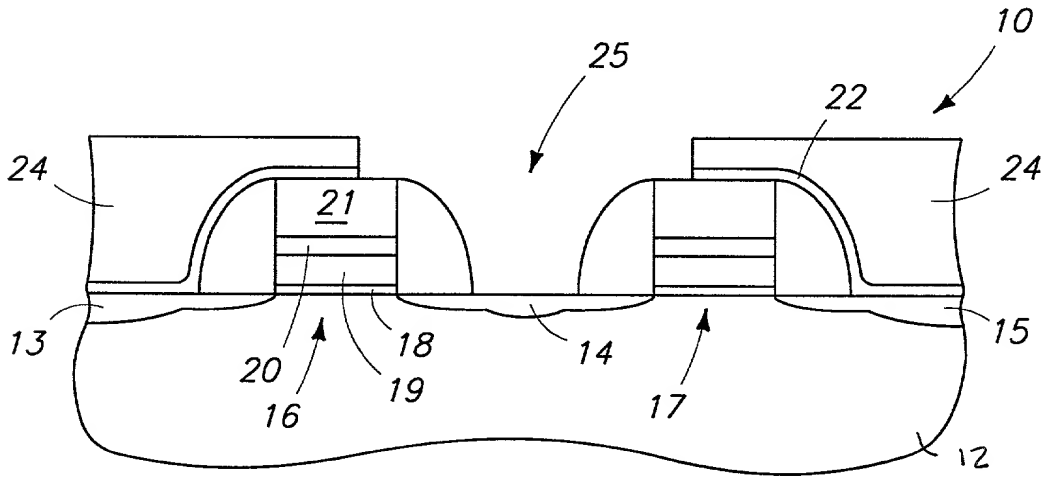


Fig. 1



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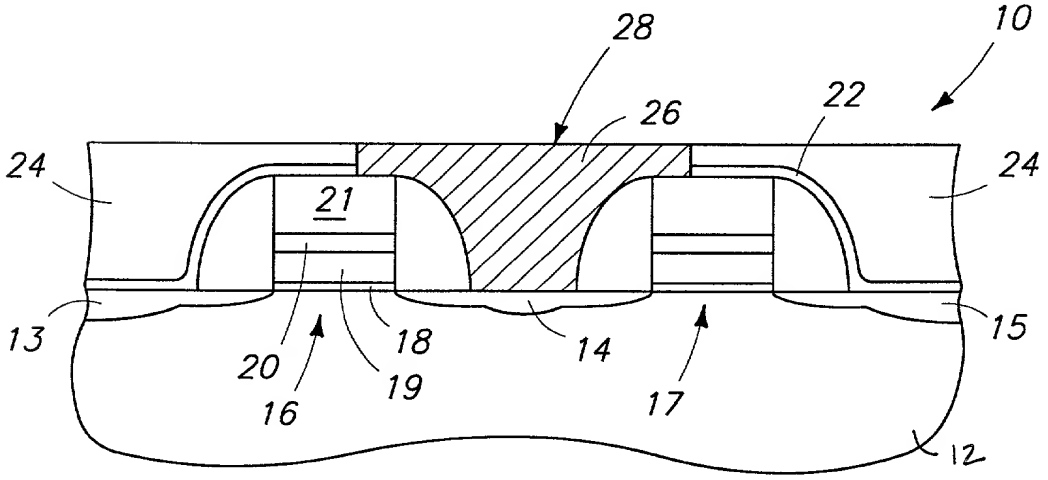

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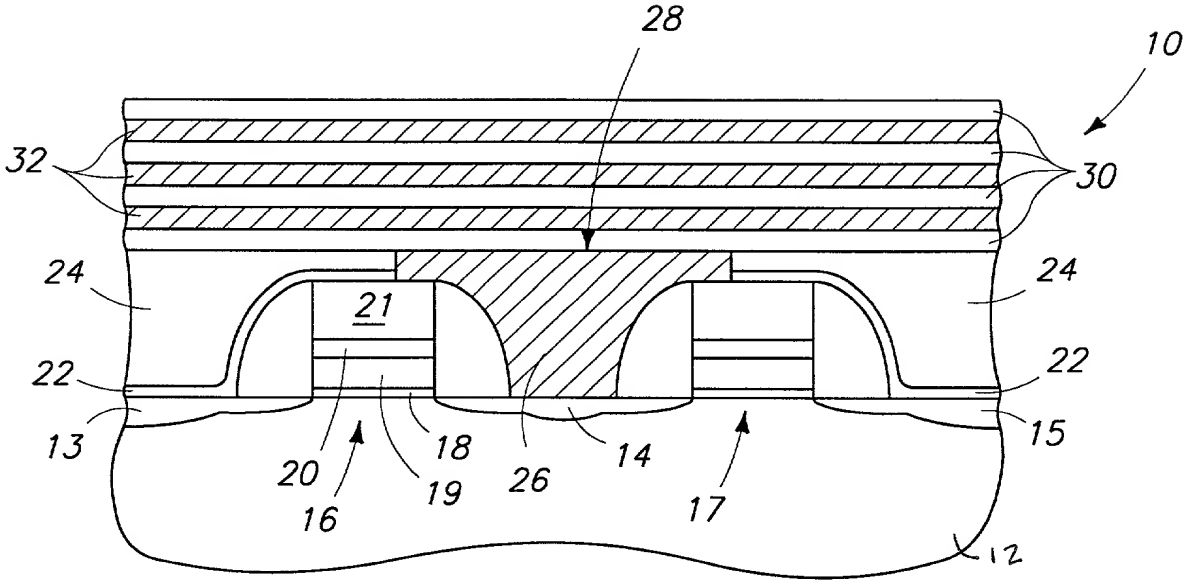

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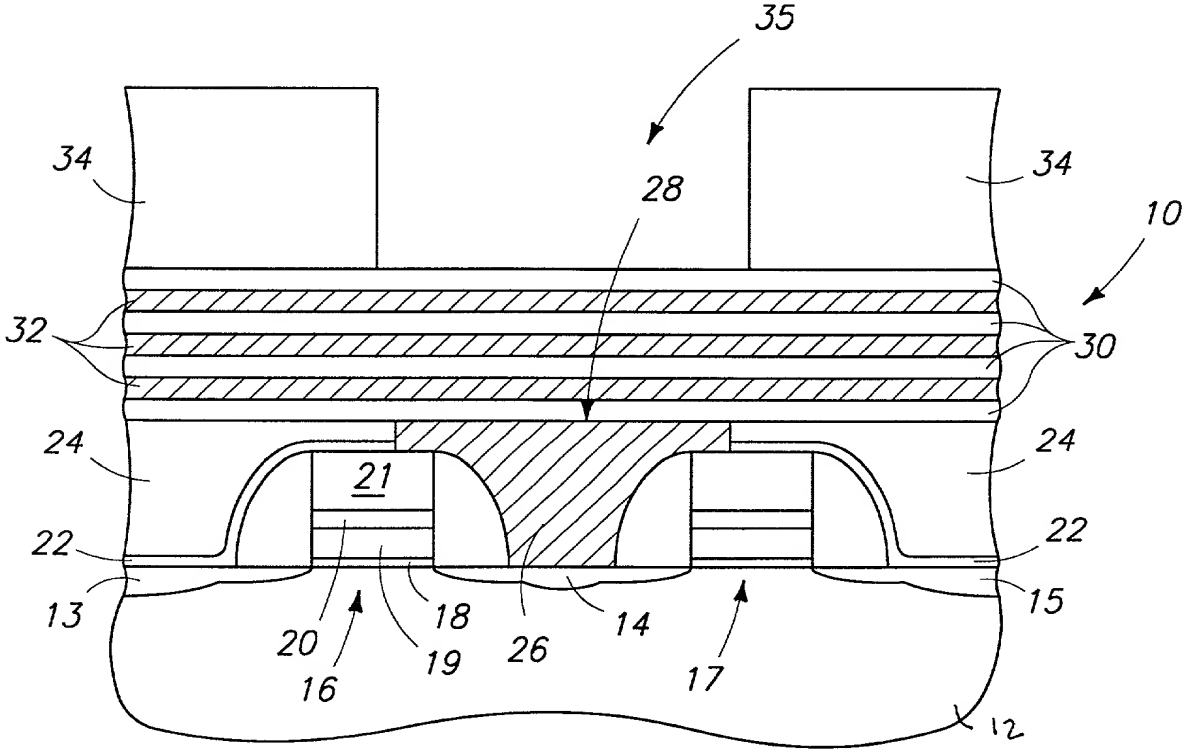

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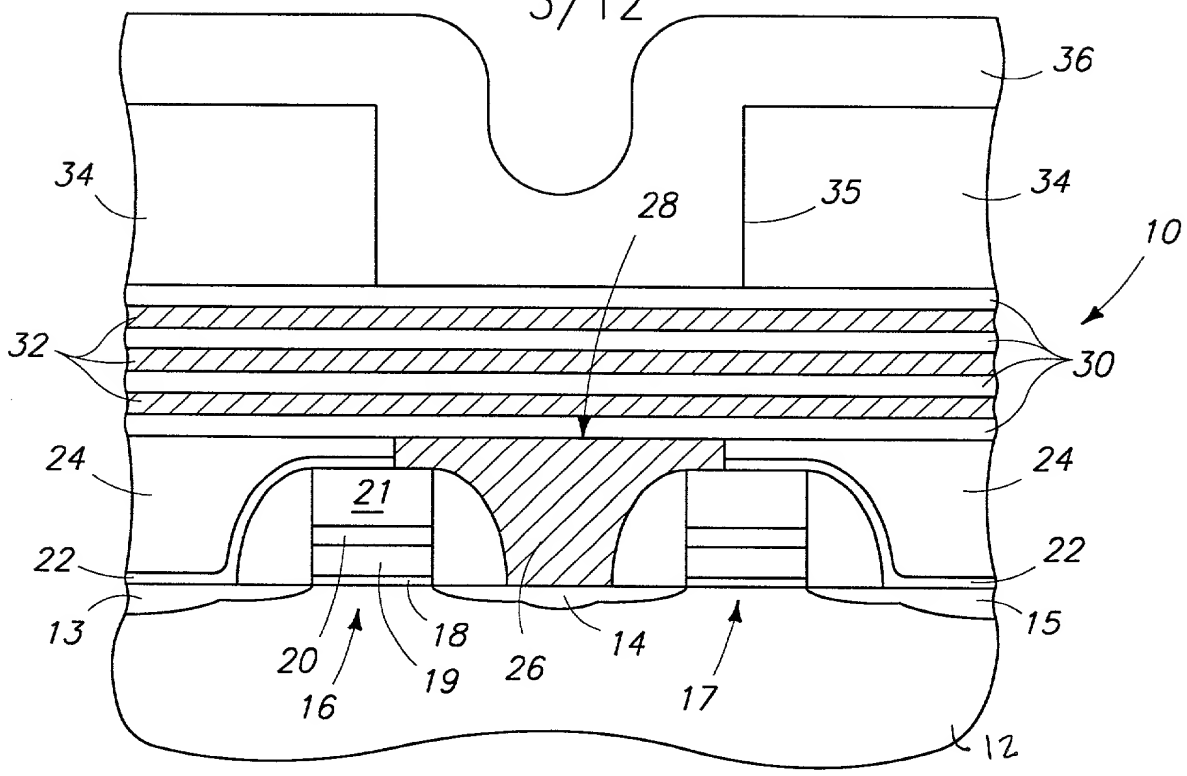
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Fig 6

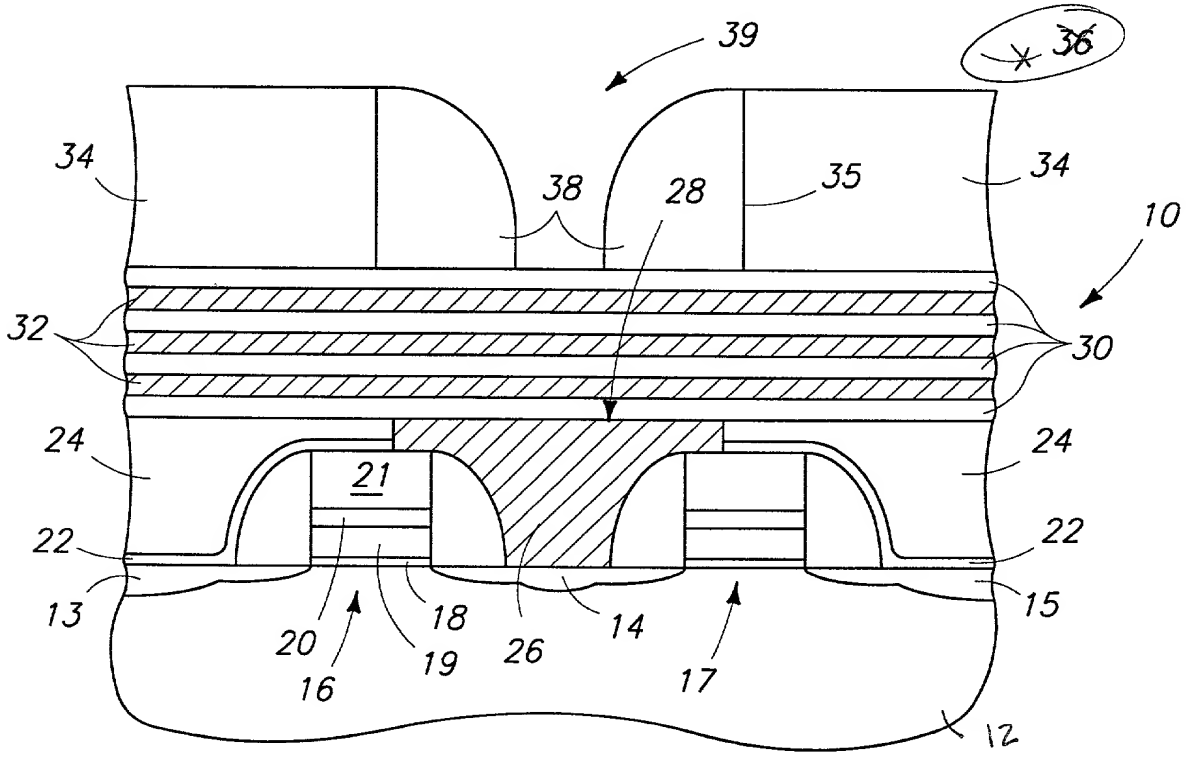
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Fig 7

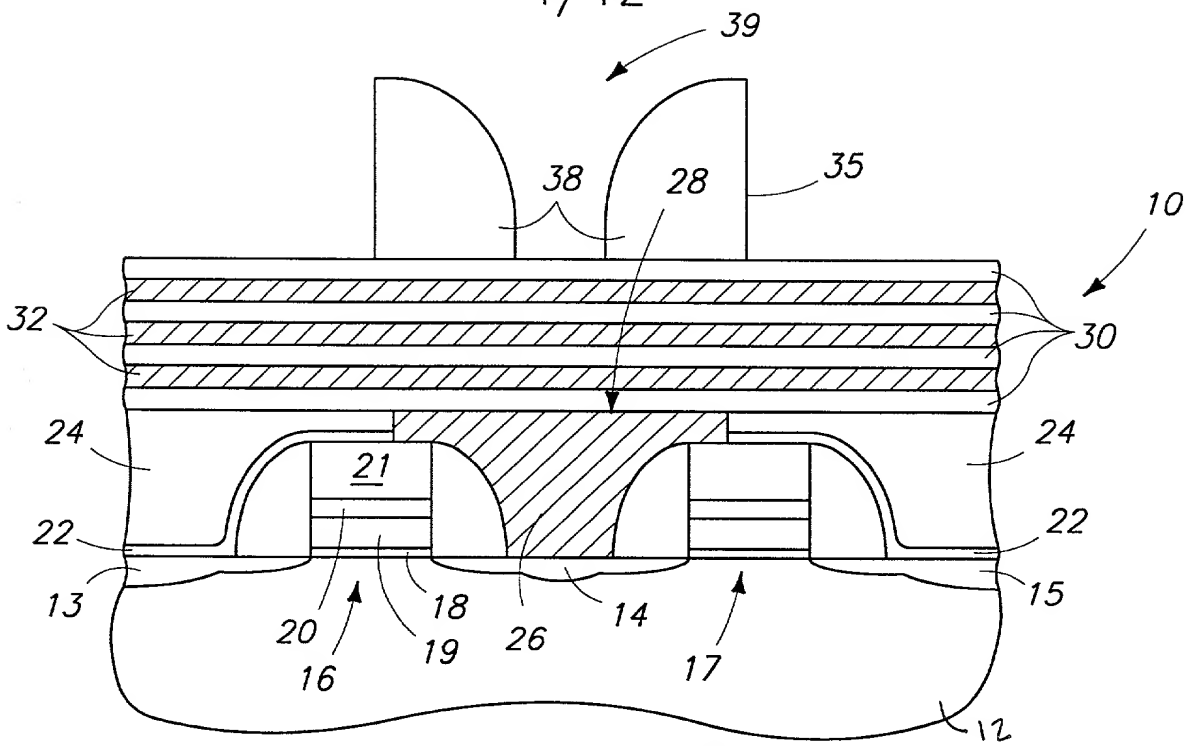
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Fig 8

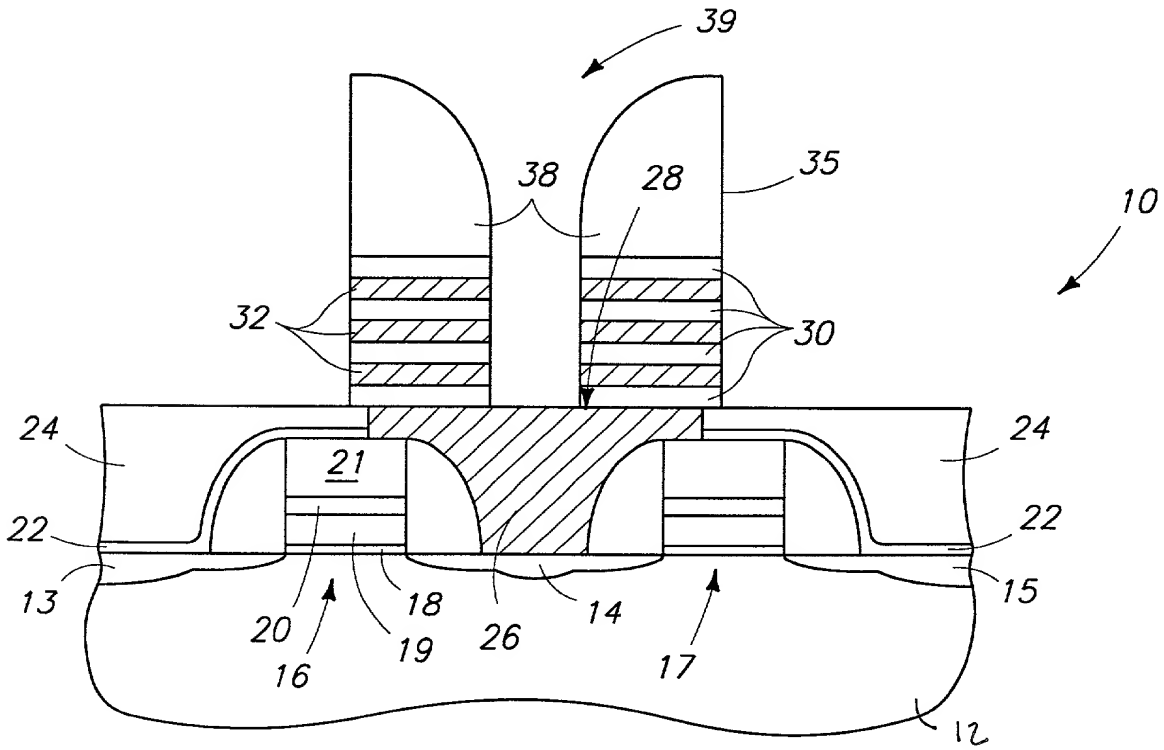
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Fig 9

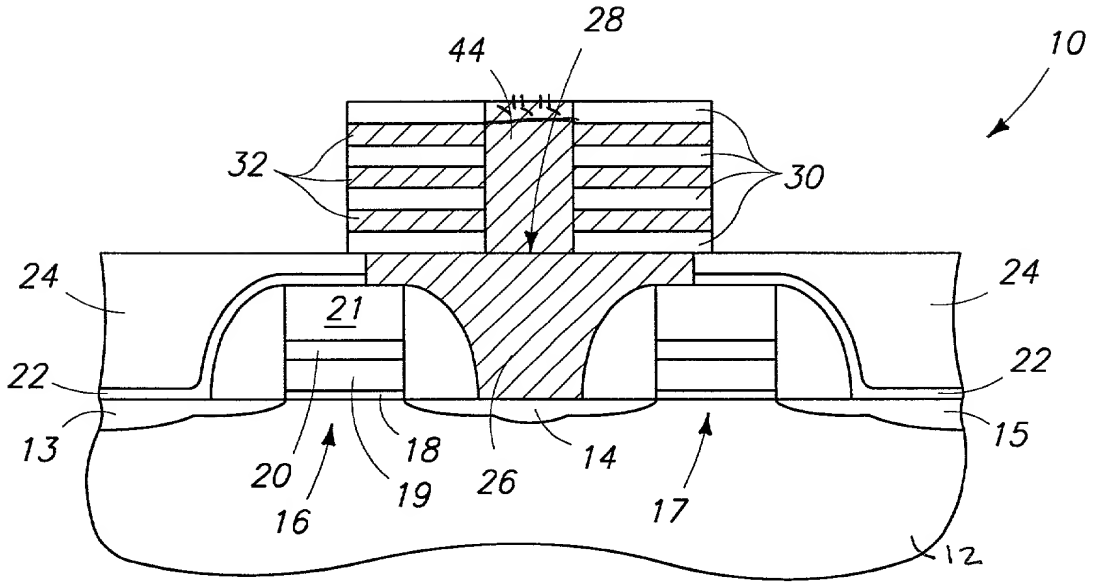
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Fig. 11

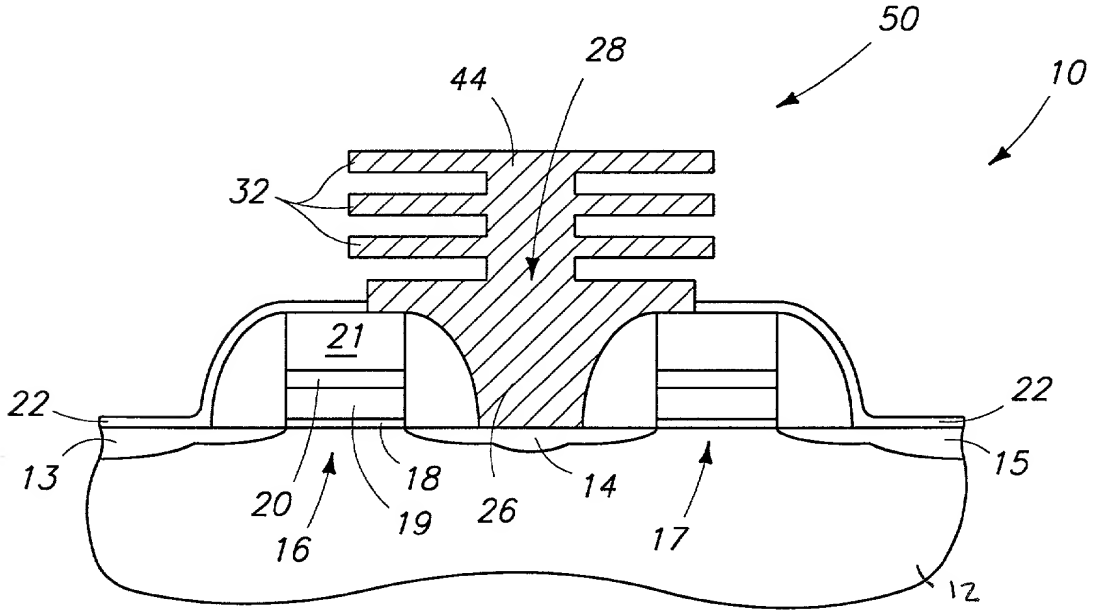
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Fig. 12

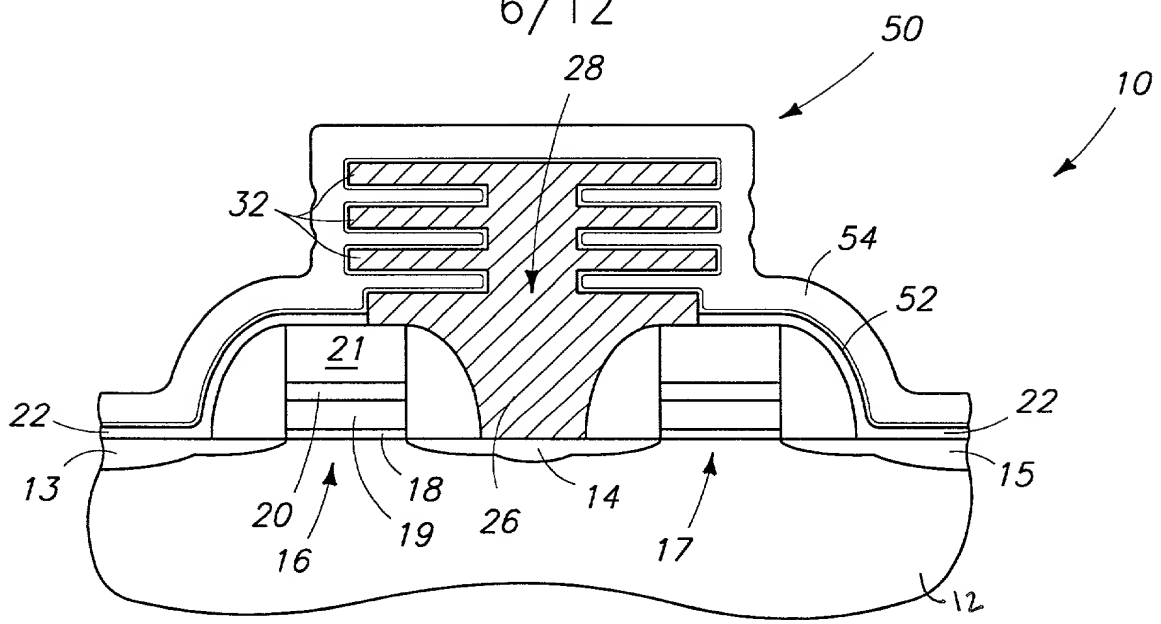

Fig 12

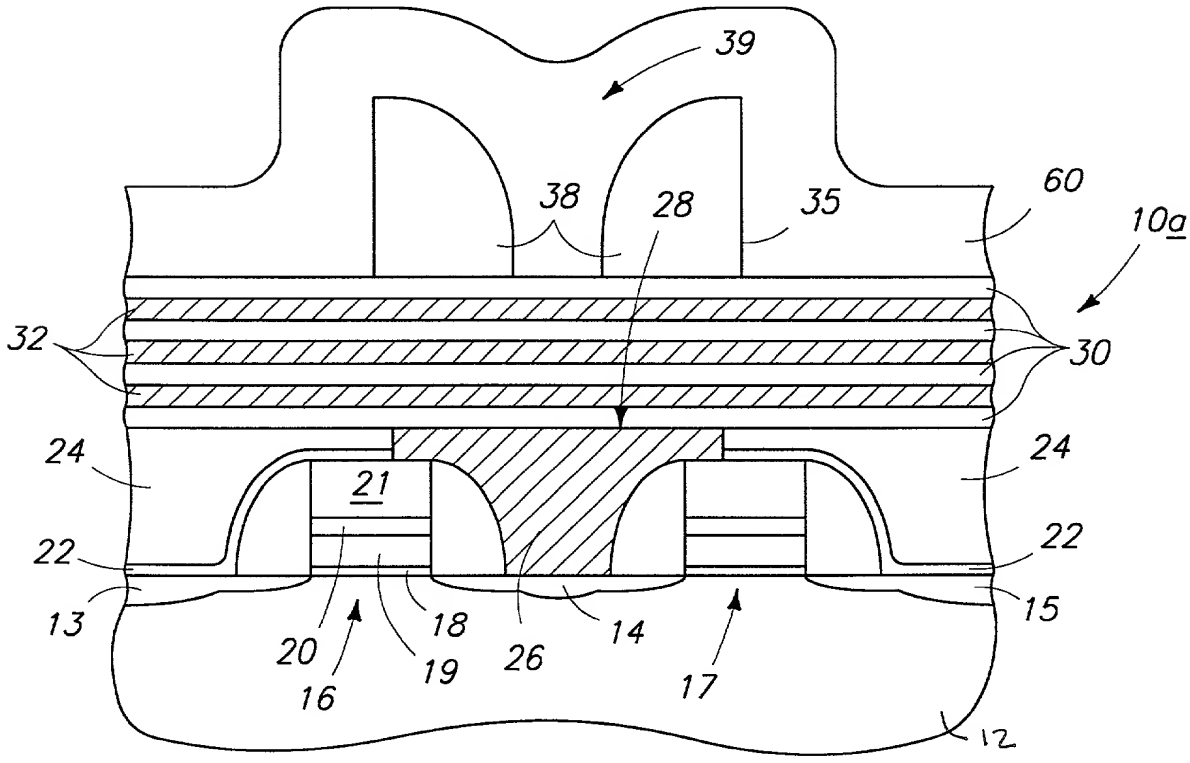

Fig 13

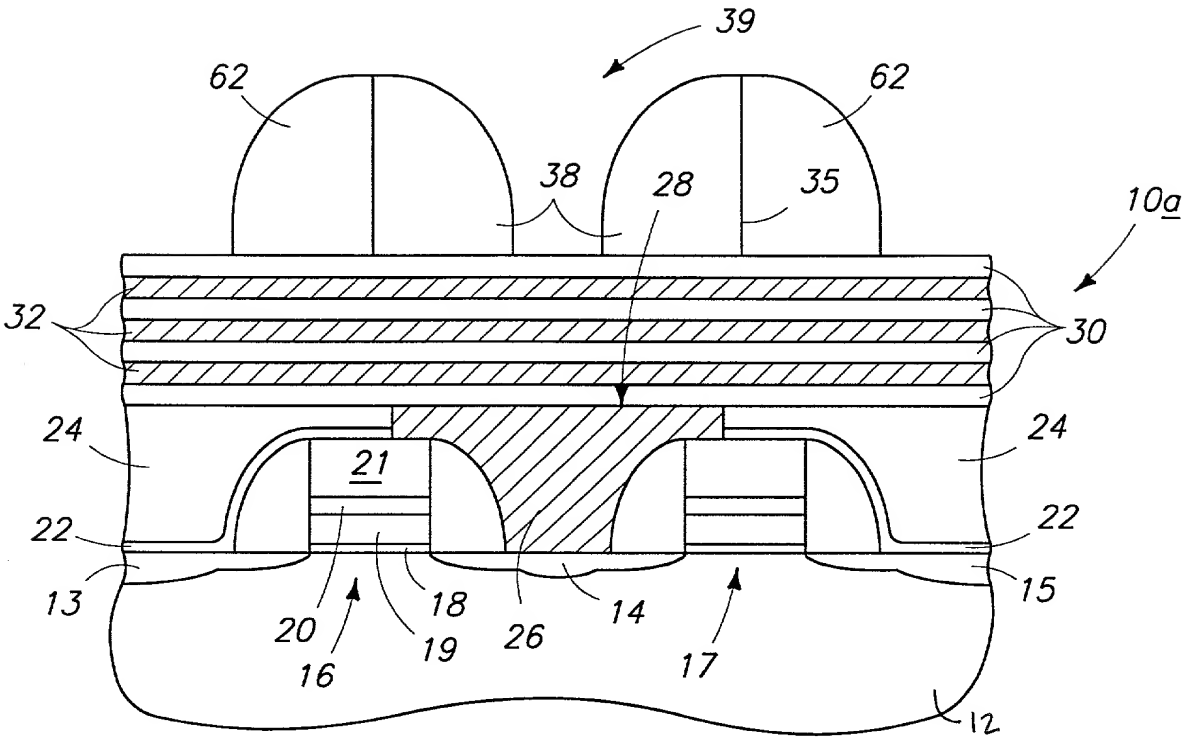

Fig. 11a

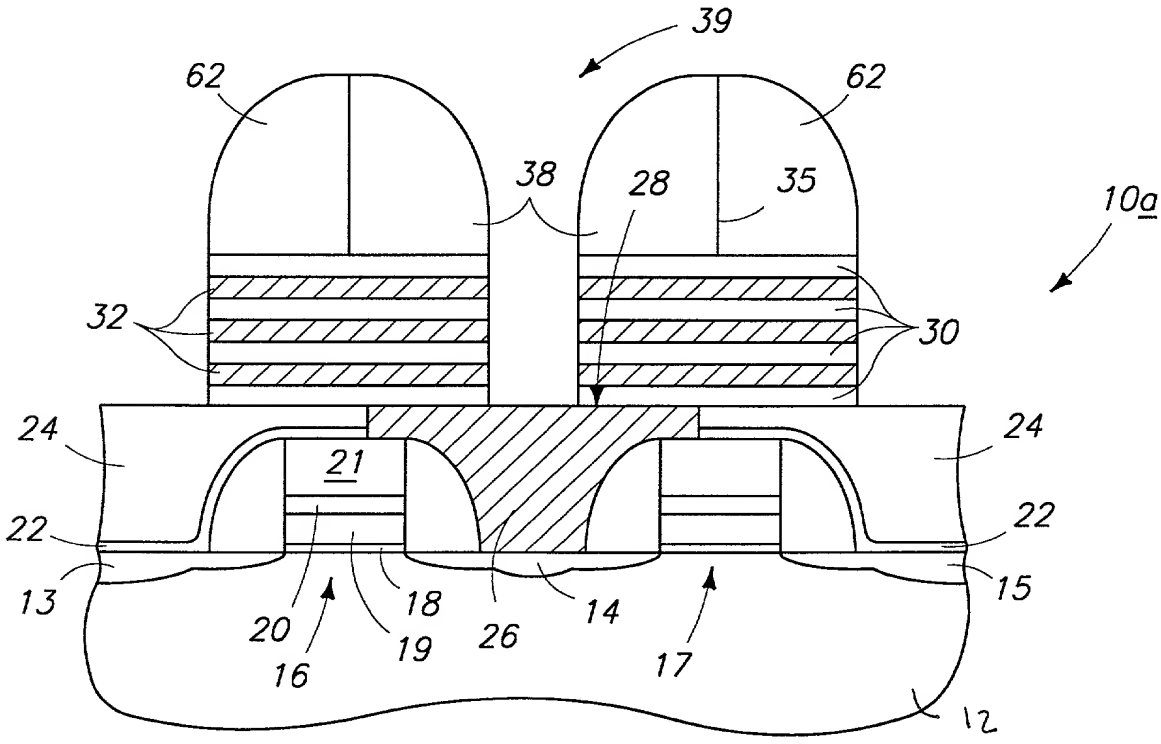

Fig. 11b

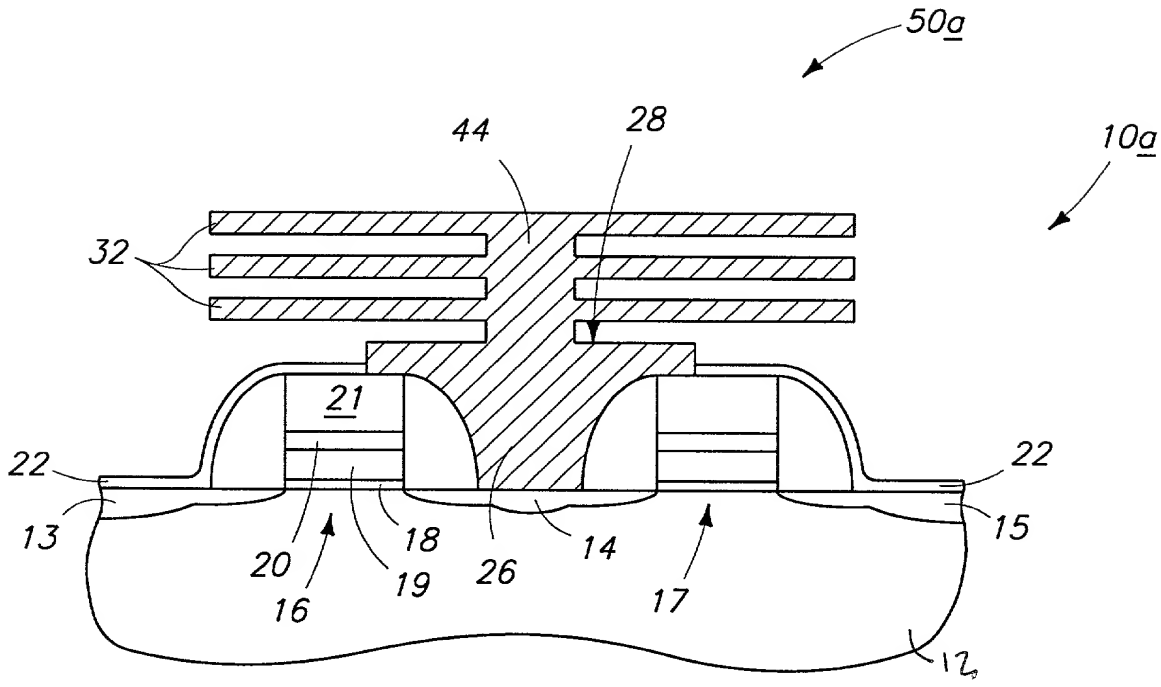

Fig 16

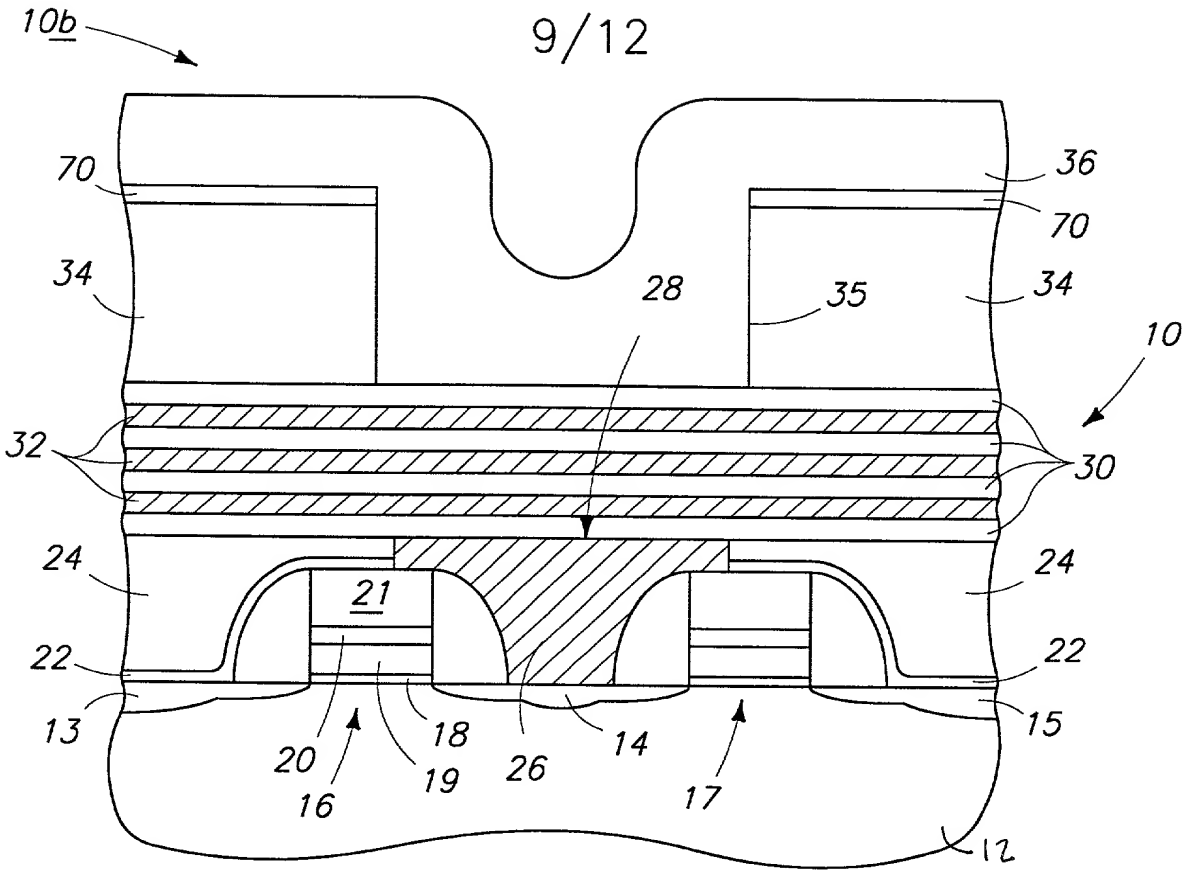
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Fig. 17

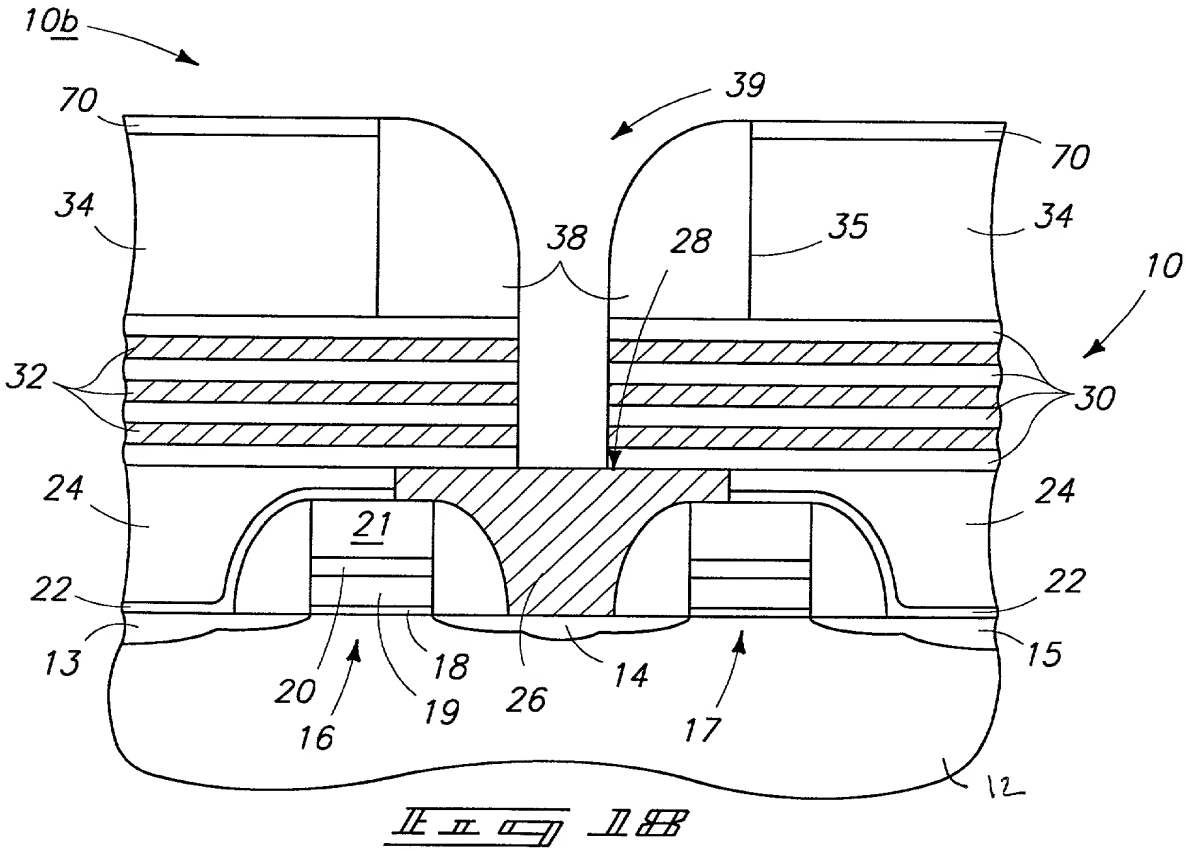
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Fig. 18

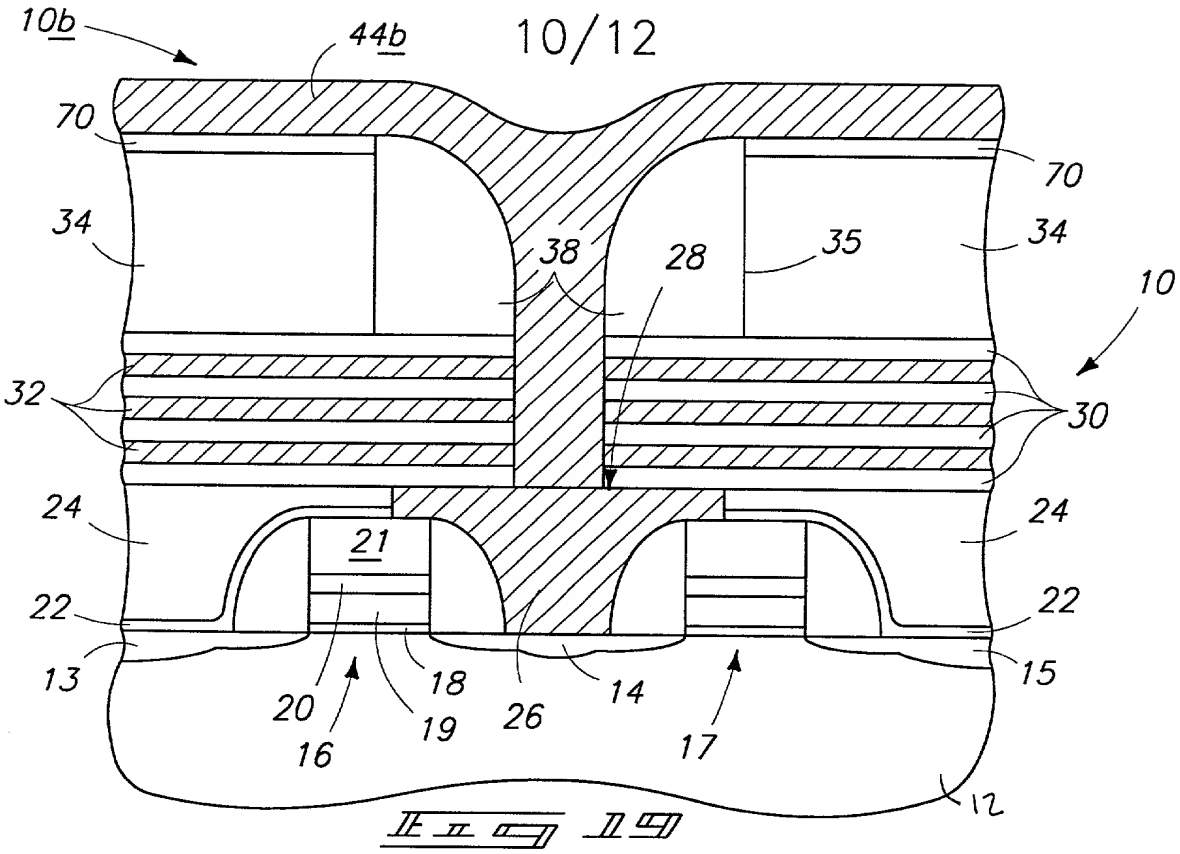
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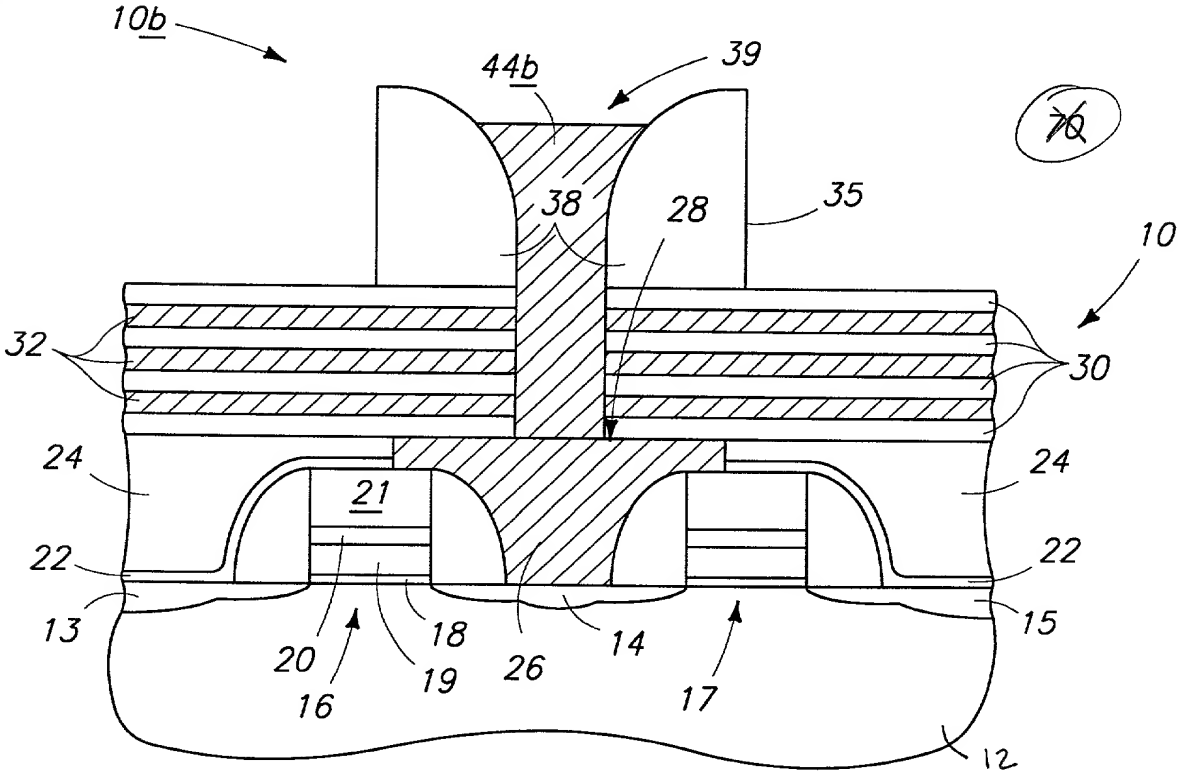
Fig 19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44b
39
70
38
28
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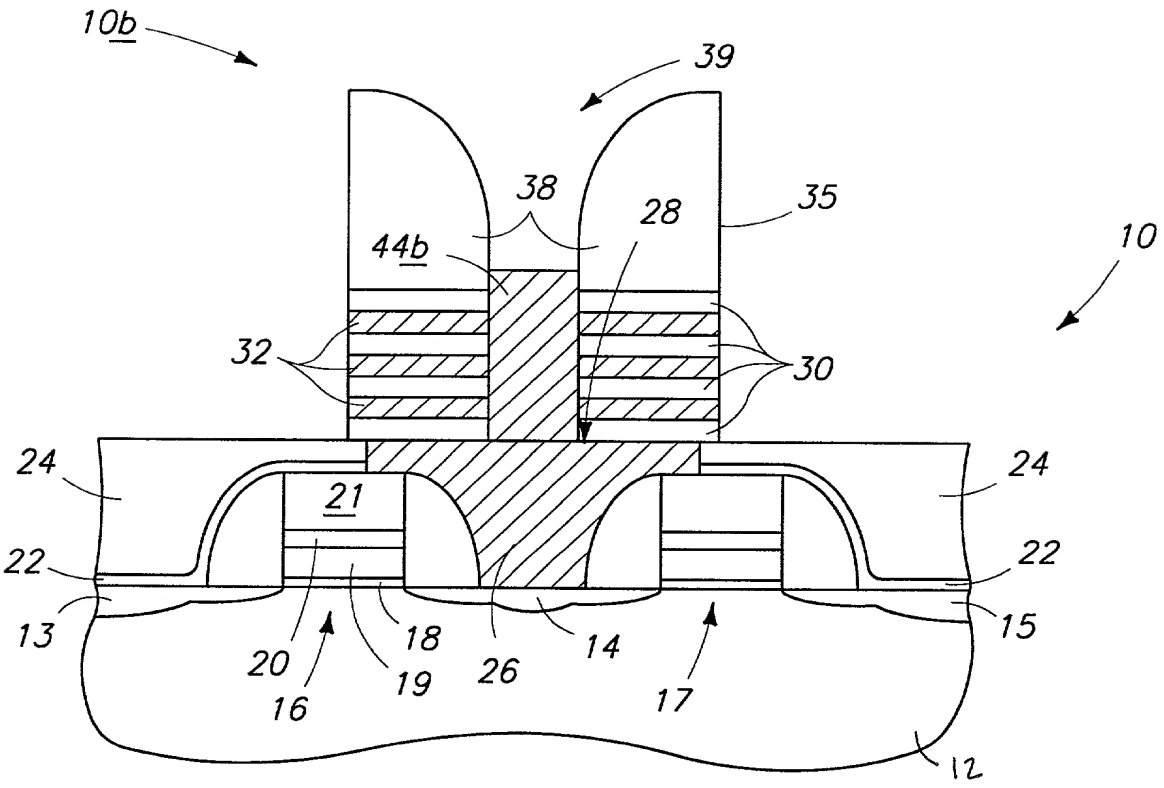
12

Fig 20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44b
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Fig 2 II

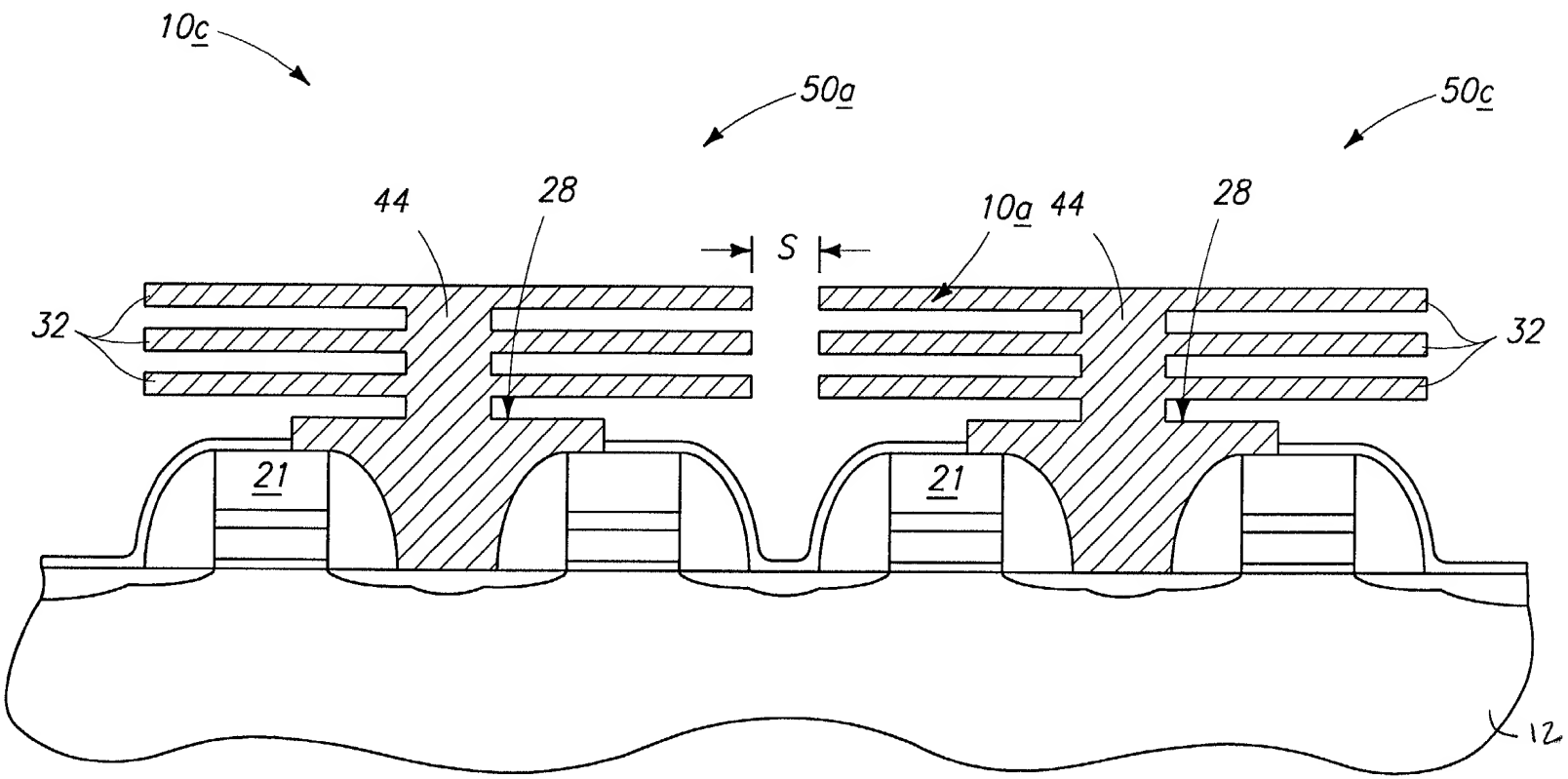

Fig 2